Features

- **Supply Voltage 5V (Typically)**
- **Very Low Power Consumption: 150 mW (Typically) for –1 dBm Output Level**
- **Very Good Sideband Suppression by Means of Duty Cycle Regeneration of the LO Input Signal**
- **Phase Control Loop for Precise 90° Phase Shifting**
- **Power-down Mode**
- **Low LO Input Level: –10 dBm (Typically)**
- **50-Ω Single-ended LO and RF Port**
- **LO Frequency from 100 MHz to 1 GHz**
- **SO16 Package**

Benefits

- **No External Components Required for Phase Shifting**
- **Adjustment Free, Hence Saves Manufacturing Time**
- **Only Three External Components Necessary, this Results in Cost and Board Space Saving**

Electrostatic sensitive device.
Observe precautions for handling.

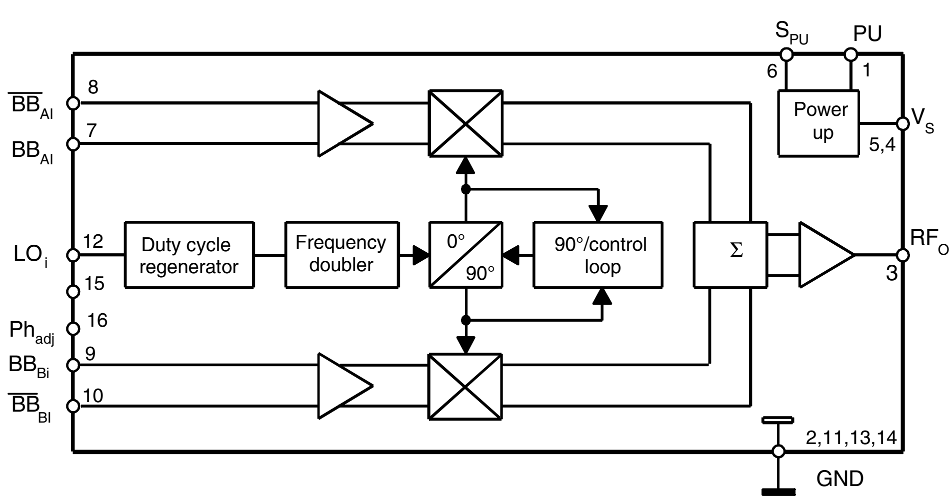
1000-MHz Quadrature Modulator

U2790B

1. Description

The U2790B is a 1000-MHz quadrature modulator using Atmel®'s advanced UHF process. It features a frequency range from 100 MHz up to 1000 MHz, low current consumption, and single-ended RF and LO ports. Adjustment-free application makes the direct converter suitable for all digital radio systems up to 1000 MHz, e.g., GSM, ADC, JDC.

Figure 1-1. Block Diagram



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2. Pin Configuration

Figure 2-1. Pinning SO16

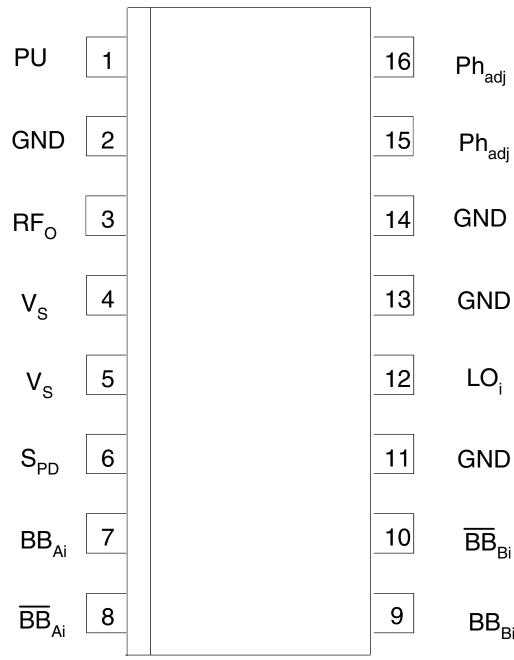


Table 2-1. Pin Description

Pin	Symbol	Function
1	PU	Power-up input
2, 11, 13, 14	GND	Ground
3	RF_o	RF output
4, 5	V_S	Supply voltage
6	S_{PU}	Settling time power-up
7	BB_{Ai}	Baseband input A
8	$\overline{BB}_{Ai}$	Baseband input A inverse
9	BB_{Bi}	Baseband input B
10	$\overline{BB}_{Bi}$	Baseband input B inverse
12	LO_i	LO input
15, 16	Ph_{adj}	Phase adjustment (not necessary for regular applications)

3. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_S	6	V
Input voltage	V_i	0 to V_S	V
Junction temperature	T_j	125	°C
Storage temperature range	T_{Stg}	–55 to +125	°C

4. Operating Range

Parameters	Symbol	Value	Unit
Supply voltage range	V_S	4.5 to 5.5	V
Ambient temperature range	T_{amb}	–40 to +85	°C

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SO16	R_{thJA}	110	K/W

6. Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 5V, T_{amb} = 25°C, referred to test circuit, system impedance Z_O = 50Ω, f_{LO} = 900 MHz, P_{LO} = –10 dBm, V_{BBi} = 1 V_{pp} differential.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Supply voltage range		4, 5	V_S	4.5		5.5	V	A
1.2	Supply current		4, 5	I_S	24	30	37	mA	A
2	**Baseband Inputs**								
2.1	Input-voltage range (differential)		7-8, 9-10	V_{BBi}		1000	1500	mV_{pp}	D
2.2	Input impedance (single ended)			Z_{BBi}		3.2		kΩ	D
2.3	Input-frequency range(5)			f_{BBi}	0		250	MHz	D
2.4	Internal bias voltage			V_{BBb}	2.35	2.5	2.65	V	A
2.5	Temperature coefficient			TC_{BB}		0.1	<1	mV/°C	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. The required LO level is a function of the LO frequency.
2. In reference to an RF output level ≤ –1 dBm and I/Q input level of 400 mV_{pp} differential.
3. Sideband suppression is tested without connection at pins 15 and 16. For higher requirements a potentiometer can be connected at these pins.
4. For T_{amb} = –30°C to +85°C and V_S = 4.5V to 5.5V.
5. By low impedance signal source.

6. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_S = 5V, T_{amb} = 25°C, referred to test circuit, system impedance Z_O = 50Ω, f_{LO} = 900 MHz, P_{LO} = –10 dBm, V_{BBi} = 1 V_{pp} differential.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3	**LO Input**								
3.1	Frequency range		12	f_{LOi}	50		1000	MHz	D
3.2	Input level[1]			P_{LOi}	–12	–10	–5	dBm	D
3.3	Input impedance			Z_{iLO}		50		Ω	D
3.4	Voltage standing wave ratio			$VSWR_{LO}$		1.4	2		D
3.5	Duty cycle range			DCR_{LO}	0.4		0.6		D
4	**RF Output**								
4.1	Output level		3	P_{RFo}	–5	–1	+2	dBm	B
4.2	LO suppression[2]	f_{LO} = 900 MHz f_{LO} = 150 MHz		LO_{RFo}	30 32	35 35		dB	B
4.3	Sideband suppression[2, 3]	f_{LO} = 900 MHz f_{LO} = 150 MHz		SBS_{RFo}	35 30	40 35		dB	B
4.4	Phase error[4]			P_e		<1		deg.	D
4.5	Amplitude error			A_e		< ±0.25		dB	D
4.6	Noise floor	V_{BBi} = 2V, $\overline{V}_{BBi}$ = 3V V_{BBi} = $\overline{V}_{BBi}$ = 2.5V		N_{FL}		–132 –144		dBm/Hz	D
4.7	VSWR			$VSWR_{RF}$		1.6	2		D
4.8	3rd-order baseband harmonic suppression			S_{BBH}	35	45		dB	D
4.9	RF harmonic suppression			S_{RFH}		35		dB	D
5	**Power-up Mode**								
5.1	Supply current	$V_{PU} \le 0.5V$ V_{PU} = 1V	4, 5	I_{PU}		10	1	µA	D
5.2	Settling time	C_{SPU} = 100 pF C_{LO} = 100 pF C_{RFo} = 1 nF	6 to 3	t_{sPU}		10		µs	D
6	**Switching Voltage**								
6.1	Power-on		1	V_{PUon}	4			V	D
6.2	Power-up		1	V_{PUdown}			1	V	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. The required LO level is a function of the LO frequency.
2. In reference to an RF output level ≤ –1 dBm and I/Q input level of 400 mV_{pp} differential.
3. Sideband suppression is tested without connection at pins 15 and 16. For higher requirements a potentiometer can be connected at these pins.
4. For T_{amb} = –30°C to +85°C and V_S = 4.5V to 5.5V.
5. By low impedance signal source.

7. Diagrams

Figure 7-1. Typical Single Sideband Output Spectrum at V_S = 4.5V and V_S = 5.5V, f_{LO} = 900 MHz, P_{LO} = –10 dBm, V_{BBI} = 1 V_{PP} (differential) T_{amb} = 25°C

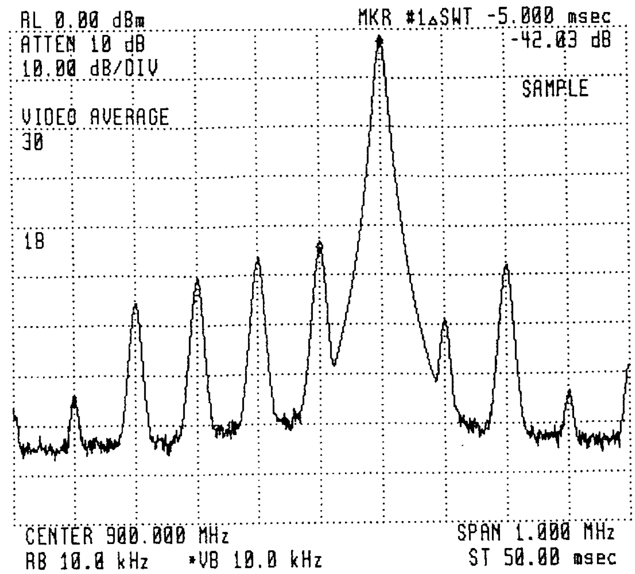


Figure 7-2. Typical GMSK Output Spectrum

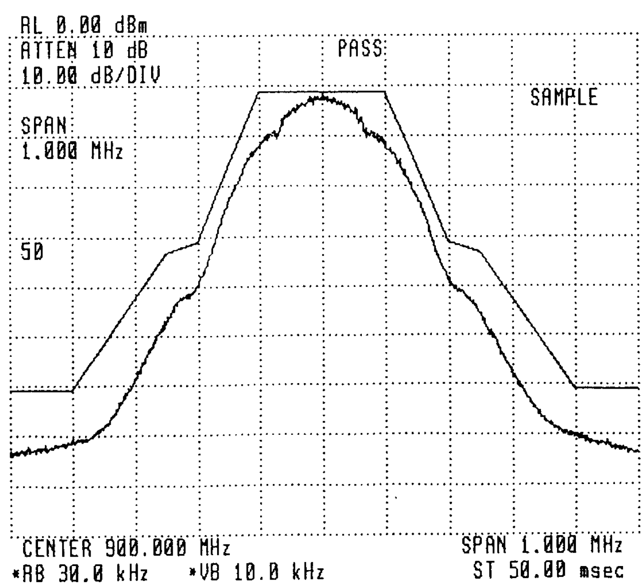


Figure 7-3. Demo Board Layout

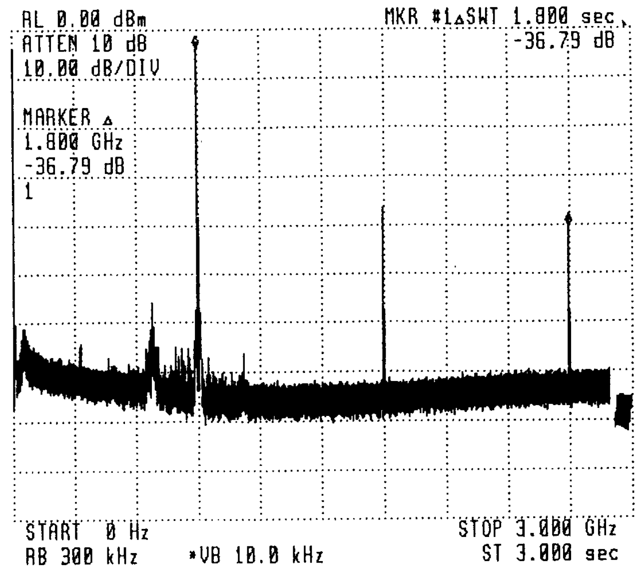


Figure 7-4. OIP3 versus T_{amb}, LO = 150 MHz, Level –20 dBm

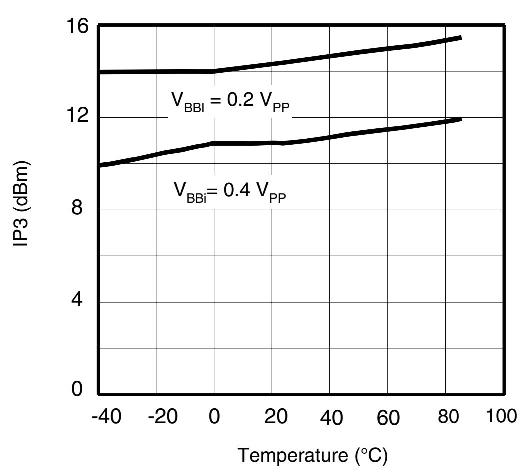


Figure 7-5. OIP3 versus T_{amb}, LO = 900 MHz, Level –10 dBm

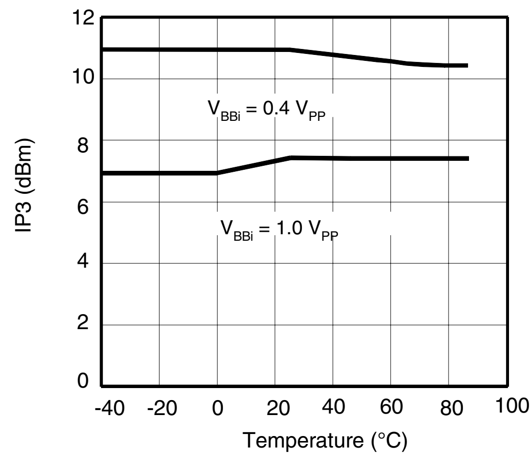


Figure 7-6. Output Power versus T_{amb}

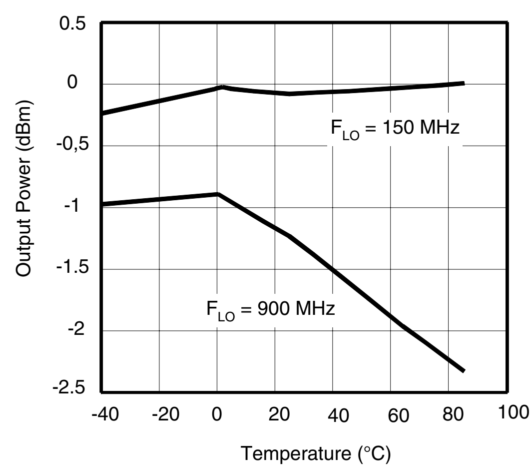


Figure 7-7. Supply Current versus T_{amb}

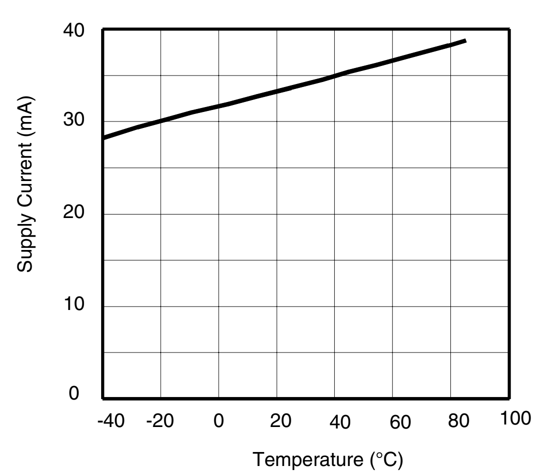


Figure 7-8. Typical S11 Frequency Response of the RF Output

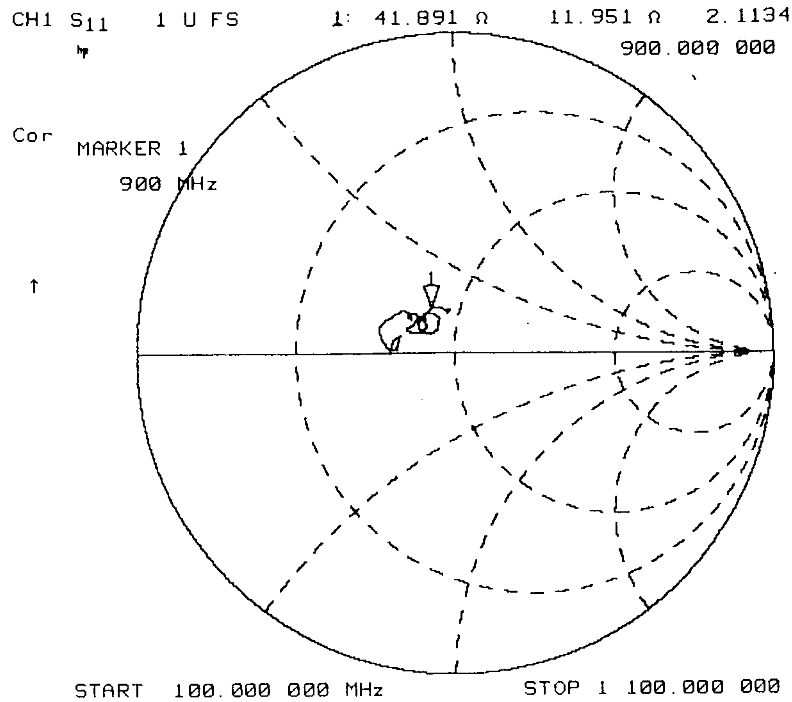


Figure 7-9. Typical VSWR Frequency Response of the RF Output

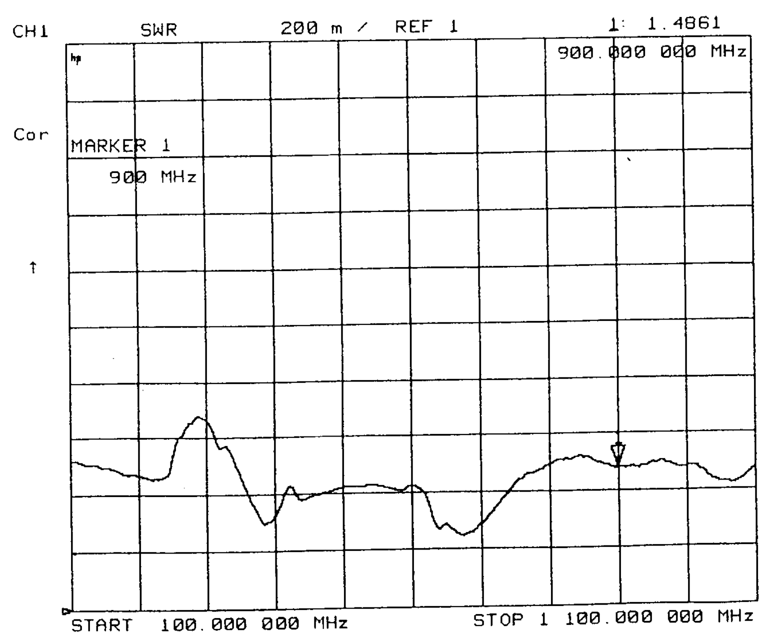


Figure 7-10. Typical S11 Frequency Response of the LO Input

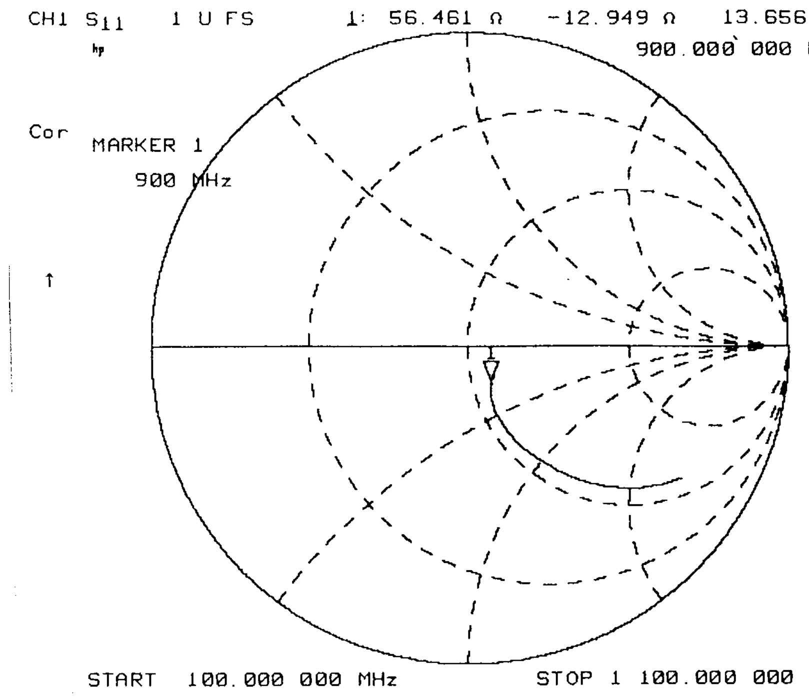


Figure 7-11. Typical VSWR Frequency Response of the LO input

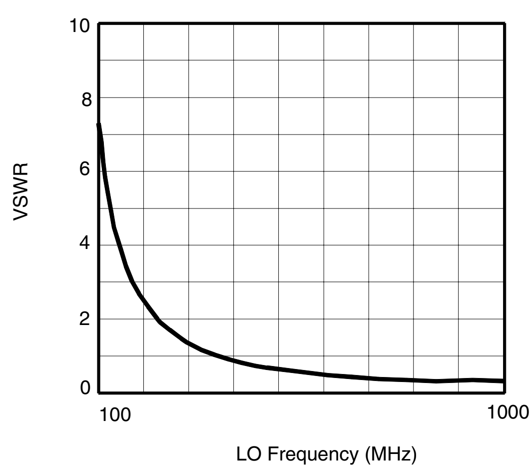


Figure 7-12. Typical Supply Current versus Temperature at V_S = 5V

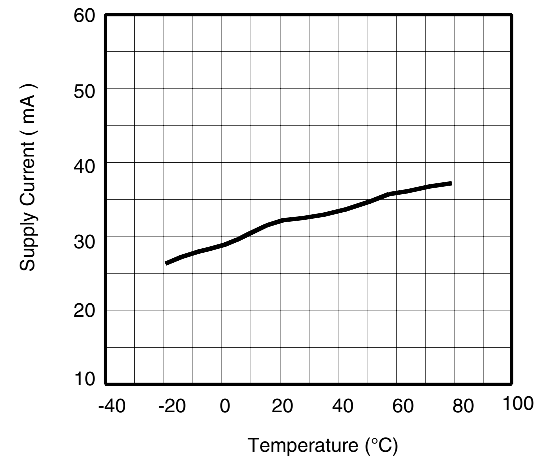


Figure 7-13. Typical Output Power versus LO-Frequency at T_{amb} = 25°C, VBBI = 230 mV_{PP} (differential)

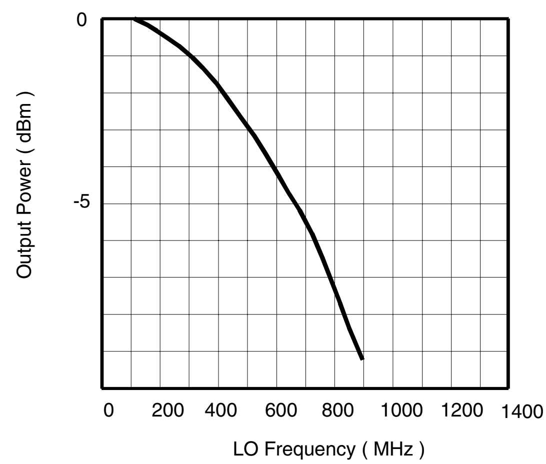


Figure 7-14. Typical required V_{BBi} Input Signal (differential) versus LO Frequency for PO = 0 dBm and P_O = –2 dBm

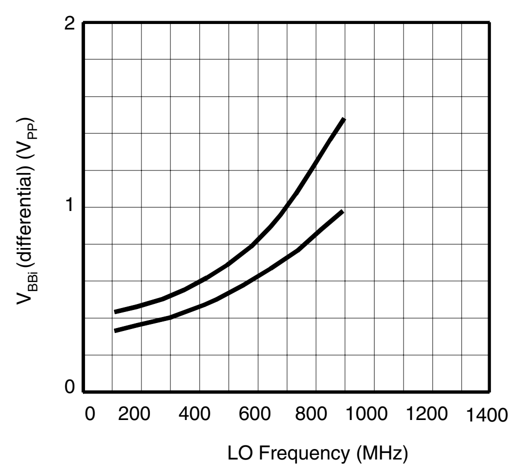


Figure 7-15. Typical useful LO Power Range versus LO Frequency at T_{amb} = 25° C

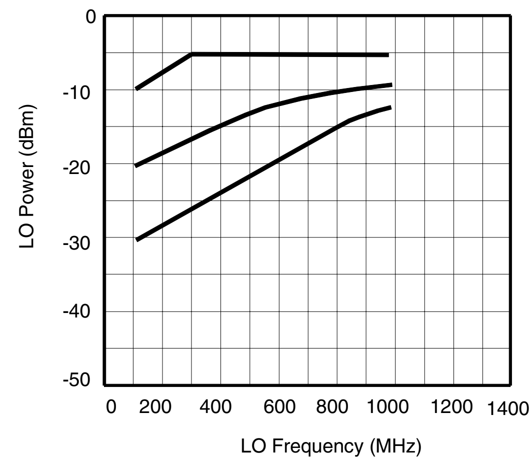


Figure 7-16. Application Circuit

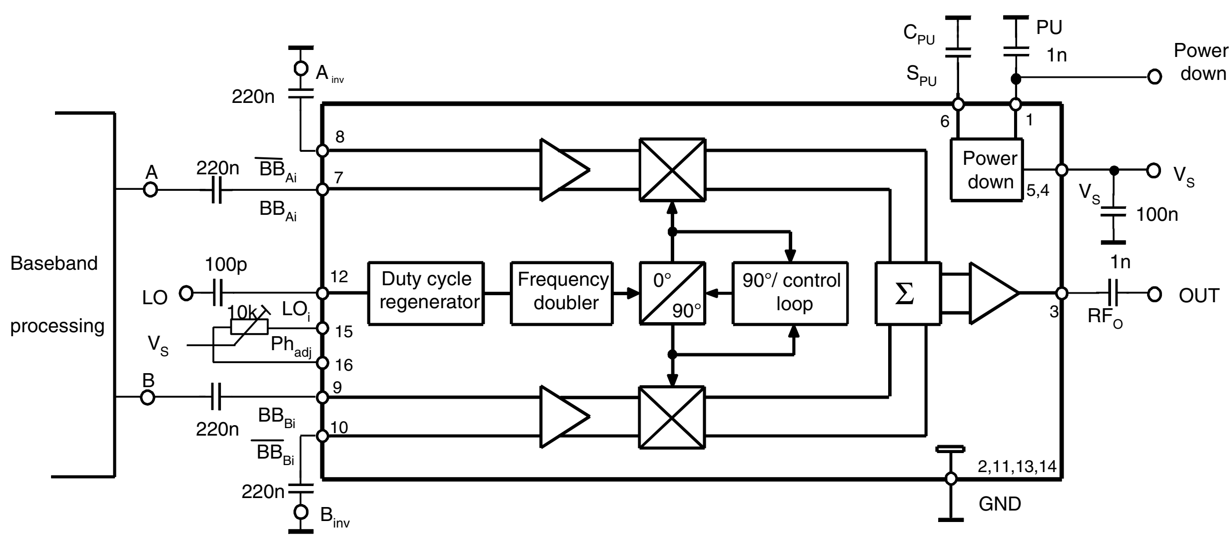
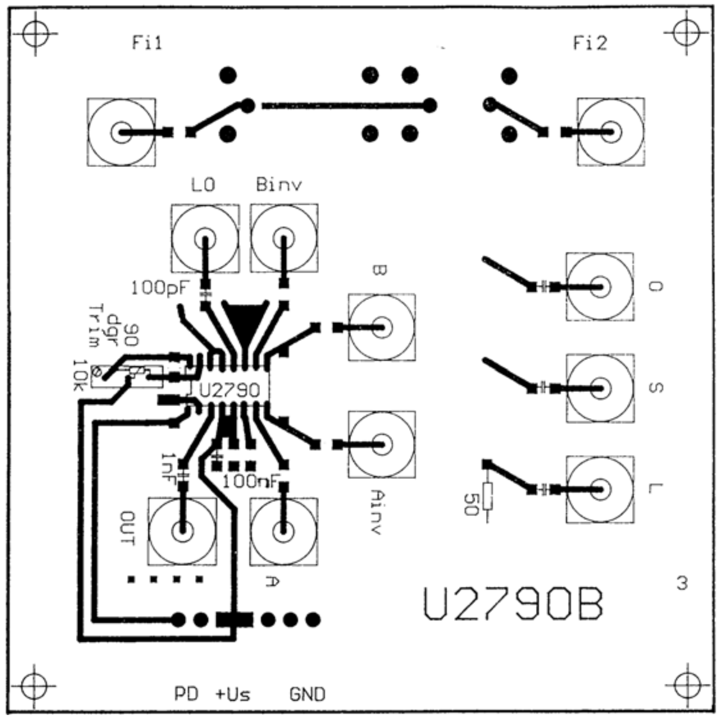


Figure 7-17. Demo Board Layout



8. Application Notes

8.1 Noise Floor and Settling Time

In order to reduce noise on the power-up control input and improve the wide-off noise floor of the 900-MHz RF output signal, capacitor C_{PU} should be connected from pin 6 to ground in the shortest possible way.

The settling time has to be considered for the system under design. For GSM applications, a value of C_{PU} = 1 nF defines a settling time, t_{sPU}, equal or less than 3 ms. This capacitance does not have any influence on the noise floor within the relevant GSM mask. For mobile applications the mask requirements can be achieved very easily without C_{PU}.

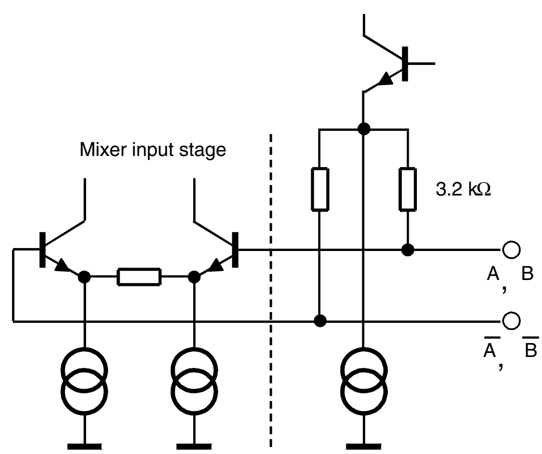
A significant improvement of the wide-off noise floor is obtainable with C_{PU} greater than 100 nF. Such values are recommended for applications where the settling time is not critical such as in base stations. Coupling capacitors for LO_i and RF_O also have a certain impact on the settling time. The values used for the measurements are CLO_i = 100 pF and C_{RFo} = 1 nF.

8.2 Baseband Coupling

The U2790B-FP (SO16) has an integrated biasing network which allows AC coupling of the baseband signal at a low count of external components. The bias voltage is 2.5V ±0.15V.

Figure 7-17 shows the baseband input circuitry with a resistance of 3.2 kΩ for each asymmetric input. The internal DC offset between A and A, and B and B is typically < ±1 mV with a maximum of ±3 mV. DC coupling is also possible with an external DC voltage of 2.5 ±0.15V.

Figure 8-1. Baseband Input Circuitry



RF Output Circuitry LO Input Circuitry

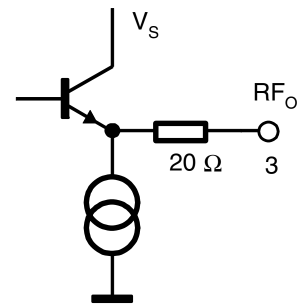
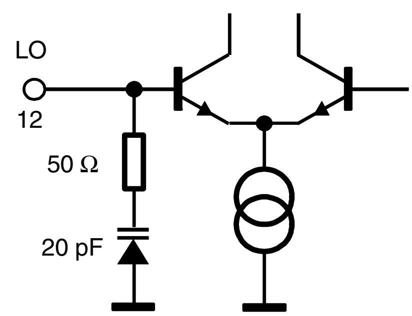


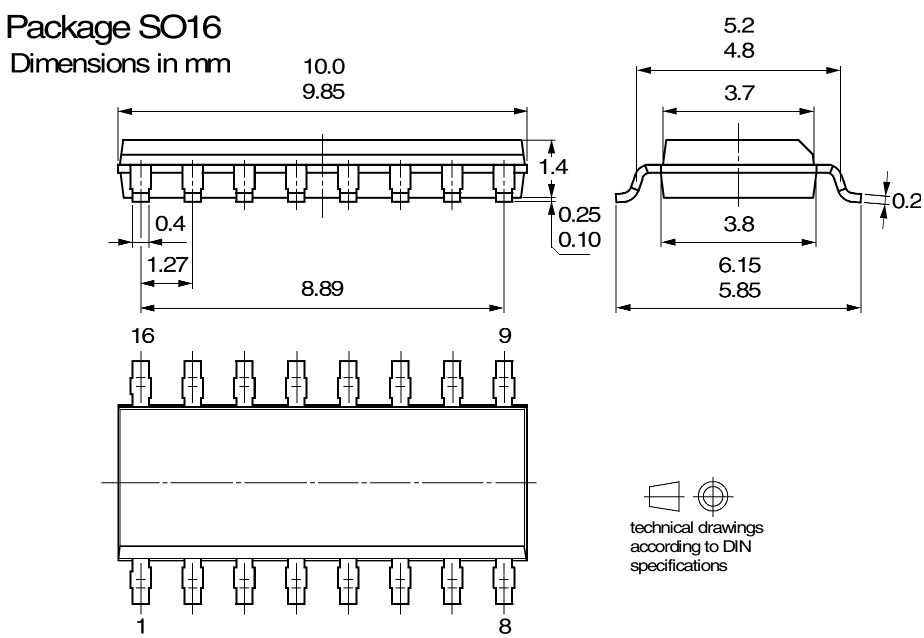
Figure 8-2. LO Input Circuitry



9. Ordering Information

Extended Type Number	Package	Remarks
U2790B-NFPH	SO16	Tube, Pb-free
U2790B-NFPG3H	SO16	Taped and reeled, Pb-free

10. Package Information



11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4583D-CELL-07/06	• Page 3, Abs. Max.Ratings table: Storage temperature values changed • Page 2, Pin Description table: symbol of Pins 8 and 10 changed • Put datasheet in a new template

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