# HV56020

## Dual High Voltage Op Amp with Step-Up Converter and Power MOSFET

### Features

- **Dual High Voltage Operational Amplifiers**
  - Up to +225V
  - 40 mA Minimum Peak Output Sink/Source Current
  - Output Voltage Comparators for Short Circuit Detection
  - 124 Hz, –3 dB Bandwidth with 0.22 µF Load
- **DC-to-DC Step-Up Converter**
  - Single Input Voltage Supply $V_{IN}$: 2.7V to 5.5V
  - Overvoltage Protection
  - Undervoltage Protection
  - Short Circuit Protection
  - Low Current Standby Mode
  - Temperature Sensor
  - Power-ON Reset
  - 24 MHz SPI Interface
- **Power MOSFET**
  - 60V $BV_{DSS}$
  - 10 mΩ On Resistance

### Applications

- Haptic Drivers
- Power Amplifiers

### Related Devices

- HV56022 Dual High Voltage Operational Amplifiers

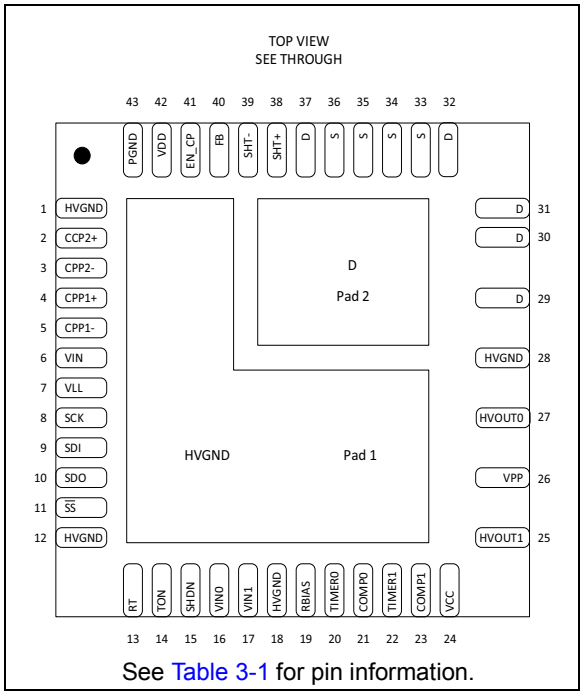
### Description

The HV56020 is a Multi-Chip Module (MCM) driver solution designed for Haptic Applications. The IC consists of three devices: (1) Dual High Voltage Operational Amplifiers, (2) a DC-to-DC Controller, and (3) a Power MOSFET. The Op Amps are designed to drive haptic (piezo) actuators at 225V with 40 mA minimum source/sink current. The DC-to-DC Controller and the power MOSFET along with an external transformer generate the voltage supply for the High Voltage Op Amps using a Non-Isolated Flyback configuration.

The HV56020 includes ample protection circuitry: Over/Undervoltage Protection, Output Short Circuit Protection (DC-to-DC), Temperature Sensor and Output Voltage Comparators for load Short Circuit Detection.

### Package Type

7 mm x 7 mm 43-Lead VQFN




See Table 3-1 for pin information.

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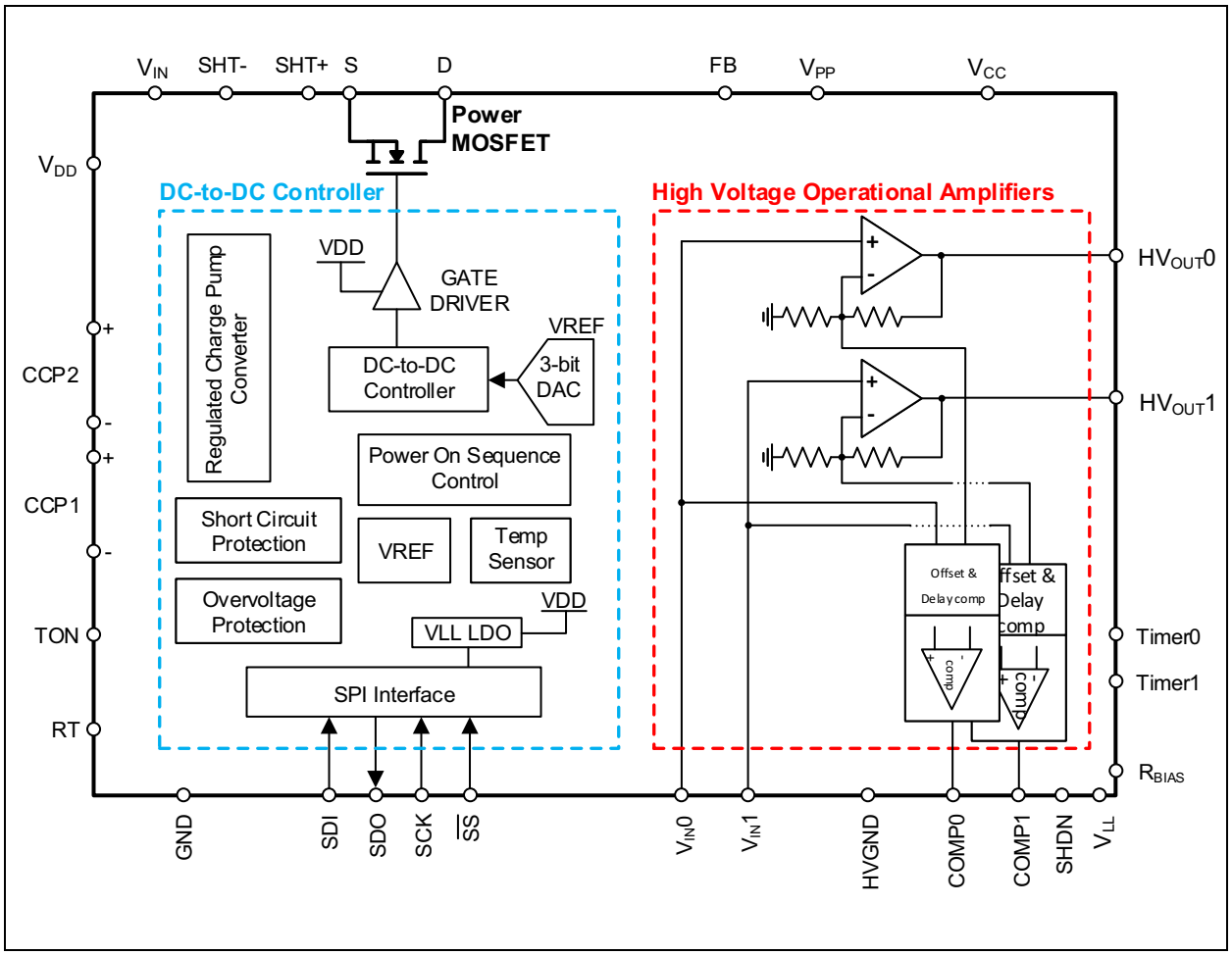
## Block Diagram





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# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

$V_{LL}$, Low Voltage Logic Supply.....-0.3V to 5.5V
$V_{IN}$0,1, High Voltage Op Amps Inputs.....-0.3V to 5.5V
$V_{IN}$, Converter Input Voltage Supply.....-0.3V to 6.0V
EN_CP, Enable Charge Pump Input Voltage.....-0.3V to 6.0V
$V_{DD}$, Low Output Voltage Supply.....-0.3V to 8.0V
$V_{CC}$, Low Voltage Supply for High Voltage Op Amps.....-0.3V to 8.0V
$V_{PP}$, High Voltage Supply for Op Amps.....-0.3V to 250V
Storage Temperature.....-55°C to +150°C
Operating Junction Temperature.....0°C to +125°C

**† Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **DC-TO-DC CONTROLLER** | | | | | | |
| Charge Pump Supply Voltage | $V_{IN}$ | 2.7 | 3.3 | 5.5 | V | |
| Logic Supply Voltage | $V_{LL}$ | 3.0 | 3.3 | 3.6 | V | Internal LDO |
| High-Level Input Logic Voltage | $V_{IH}$ | 2.0 | — | $V_{LL}$ | V | |
| Low-Level Input Logic Voltage | $V_{LL}$ | 0 | — | 0.8 | V | |
| **HIGH VOLTAGE OPERATIONAL AMPLIFIERS** | | | | | | |
| High Voltage Supply | $V_{PP}$ | 50 | — | 225 | V | |
| Low Voltage Supply | $V_{CC}$ | 6.0 | 6.5 | 7.0 | V | |
| Inputs for High Voltage Op Amps | $V_{IN}$0,1 | 0 | — | 2.98 | V | |

## POWER SEQUENCE

### Power-Up Sequence:

1. Connect ground
2. Set all driver inputs to low
3. Apply $V_{IN}$
4. Enable $V_{DD}$ ($V_{CC}$)
5. Set all converter inputs to a known state
6. Enable $V_{PP}$

### Power-Down Sequence:

1. Disable $V_{IN}$0 and $V_{IN}$1 (set to 0V)
2. Disable $V_{PP}$
3. Disable $V_{DD}$ ($V_{CC}$)
4. Power down $V_{IN}$
5. Disconnect ground

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## DC-TO-DC CONTROLLER: AC/DC CHARACTERISTICS

Unless otherwise specified, $T_A = T_J$ = +25°C. **Boldface** specifications apply over the full operating temperature range of $T_A = T_J$ = 0°C to +125°C. Typical values are at +25°C. EN_CP = "1", $V_{LL}$=3.3V, $V_{CC}$ = 6.5V unless otherwise specified.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Charge Pump Regulator** | | | | | | |
| Charge Pump Input Voltage | $V_{IN}$ | **2.7** | **3.3** | **5.5** | V | |
| Charge Pump Output Voltage | $V_{DD}$ | **6** | **6.5** | **7** | V | 2.7V ≤ $V_{IN}$ ≤ 5.5V, $I_{DD}$=15 mA |
| Charge Pump Output Load Current | $I_{DD}$ | 15 | — | — | mA | Depends on IC loading and external capacitor selection |
| Output Ripple Voltage | $V_{RIPPLE}$ | — | — | 80 | mV | $V_{IN}$ = 3.3V, $I_{DD}$ = 15 mA, Output Capacitance = 10 µF (**Note 1**) |
| $V_{DD}$ Undervoltage Lockout | $VDD_{UVLO}$ | **4.25** | — | **4.75** | V | Rising Edge |
| $V_{DD}$ Undervoltage Lockout Hysteresis | $VDD_{HYST}$ | — | 0.25 | — | V | Falling |
| Enable Charge Pump Input Pin | EN_CP | 0 | — | $V_{IN}$ | V | |
| Low Threshold for EN_CP Pin | $V_{IL}$(EN_CP) | 0 | — | 0.8 | V | |
| High Threshold for EN_CP Pin | $V_{IH}$(EN_CP) | 2.0 | — | $V_{IN}$ | V | |
| Pull Down Resistor at EN_CP Pin | $EN\_CP_{PD}$ | — | 500 | — | kΩ | EN_CP = 3.3V |
| Power-Down Input Current | $I_{DDPD}$ | — | -— | 5 | µA | EN_CP = 0V |
| **Clock Generation** | | | | | | |
| Minimum Switching Frequency | $f_{s,MIN}$ | 160 | 200 | 240 | kHz | RT = 400 kΩ |
| Maximum Switching Frequency | $f_{s,MAX}$ | 320 | 400 | 480 | kHz | RT = 200 kΩ |
| Clock Ramp Maximum | $V_{TS}$ | — | 3.5 | — | V | **Note 2** |
| Clock Ramp Minimum | $V_{RST}$ | — | 0.2 | — | V | **Note 2** |
| **TON Generation** | | | | | | |
| Maximum Voltage at TON | $VTON_{MAX}$ | — | — | 2.8 | V | 2.8V = 0.8$V_{TS}$ = 80% PWM Max (**Note 2**) |
| Minimum Voltage at TON | $VTON_{MIN}$ | 0 | — | — | V | 0.25$V_{TS}$ = 25% PWM Min (**Note 2**) |
| TON Generation Internal Gain | $K_{TON}$ | — | 40 | — | V/V | **Note 2** |
| **Output Voltage Feedback** | | | | | | |
| Comparator Delay | $T_{DLYCOMP}$ | — | — | 50 | ns | 10 mV Overdrive (**Note 2**) |
| **Overvoltage Protection** | | | | | | |
| OVP Set Point | $OVP_R$ | **-3%** | **1.278** | **+3%** | V | |
| OVP Hysteresis | $OVP_{HYST}$ | — | 0.36 | — | V | |
| OVP Delay Time | $OVP_{DLY}$ | — | 50 | — | ns | 100 mV Overdrive (**Note 2**) |
| **Short Circuit Protection** | | | | | | |
| Short Circuit Comparator Offset | $SH_{OFF}$ | 34 | 50 | 68 | mV | SHT_EN = 1 (SHT+ and SHT- pins) |
| **Temperature Sensor** | | | | | | |
| Temperature Threshold | $T_{TH}$ | 125 | — | 150 | °C | **Note 2** |
| Temperature Threshold Hysteresis | $T_{THHYST}$ | — | 25 | — | °C | **Note 2** |
| **Voltage Reference 3-Bit DAC** | | | | | | |
| Integral Nonlinearity | INL | — | — | ±0.5 | LSB | **Note 1** |
| Differential Nonlinearity | DNL | — | — | ±0.5 | LSB | **Note 1** |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

**2:** Design guidance only.


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## DC-TO-DC CONTROLLER: AC/DC CHARACTERISTICS (CONTINUED)

Unless otherwise specified, $T_A = T_J = +25°C$. **Boldface** specifications apply over the full operating temperature range of $T_A = T_J = 0°C$ to +125°C. Typical values are at +25°C. EN_CP = "1", $V_{LL}$=3.3V, $V_{CC}$ = 6.5V unless otherwise specified.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Code Word** | | | | | | |
| Code 000 | | — | 0.3 $V_{REF}$ | — | V | VPP READY =1 |
| Code 001 | | — | 0.4 $V_{REF}$ | — | V | |
| Code 010 | | — | 0.5 $V_{REF}$ | — | V | |
| Code 011 | | — | 0.6 $V_{REF}$ | — | V | |
| Code 100 | | — | 0.7 $V_{REF}$ | — | V | **Note 1** |
| Code 101 | | — | 0.8 $V_{REF}$ | — | V | |
| Code 110 | | — | 0.9 $V_{REF}$ | — | V | |
| Code 111 | $V_{REF}$ | **-3%** | **1.188** | **+3%** | V | VPP READY = 1 |
| **Logic Voltage Supply (Internal LDO for SPI)** | | | | | | |
| Logic Voltage Supply | $V_{LL}$ | 3.0 | 3.3 | 3.6 | V | |
| High-Level Input Logic Voltage | $V_{IH}$ | 2.0 | — | $V_{LL}$ | V | |
| Low-Level Input Logic Voltage | $V_{IL}$ | 0 | — | 0.8 | V | |
| VLL Undervoltage Lockout | $VLDO_{UVLO}$ | 2.25 | 2.5 | 2.75 | V | |
| VLL Undervoltage Lockout Hysteresis | $VLDO_{HYST}$ | — | 0.25 | — | V | |
| **SPI Interface** | | | | | | |
| Maximum SPI Clock Frequency | SCK | 24 | — | — | MHz | 3.3V Input Logic |
| Logic Input Rise and Fall Time | $t_r$, $t_f$ | — | 5 | — | ns | **Note 1** |
| Source Current by Standard I/O Pin | Isource | 10 | — | — | mA | **Note 2** |
| Sink Current by Standard I/O Pin | Isink | 10 | — | — | mA | |
| SDI Valid to SCK Setup Time | $t_1$ | 10 | — | — | ns | |
| SDI Valid to SCK Hold Time | $t_2$ | 20 | — | — | ns | |
| SCK High Time % of $1/f_{clk}$ | $t_3$ | 45 | — | 55 | % | |
| SCK Low Time % of $1/f_{clk}$ | $t_4$ | 45 | — | 55 | % | |
| $\overline{SS}$ Pulse Width | $t_5$ | 300 | — | — | ns | **Note 1** |
| LSB SCK High to $\overline{SS}$ High | $t_6$ | 10 | — | — | ns | |
| $\overline{SS}$ Low to SCK High | $t_7$ | 20 | — | — | ns | |
| SDO Propagation Delay from SCK Falling Edge | $t_8$ | 10 | — | — | ns | |
| SDO Output Valid after $\overline{SS}$ Low | $t_9$ | 20 | — | — | ns | |
| $\overline{SS}$ Inactive to SDO High Impedance | $t_{10}$ | 40 | — | — | ns | **Note 2** |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

**2:** Design guidance only.

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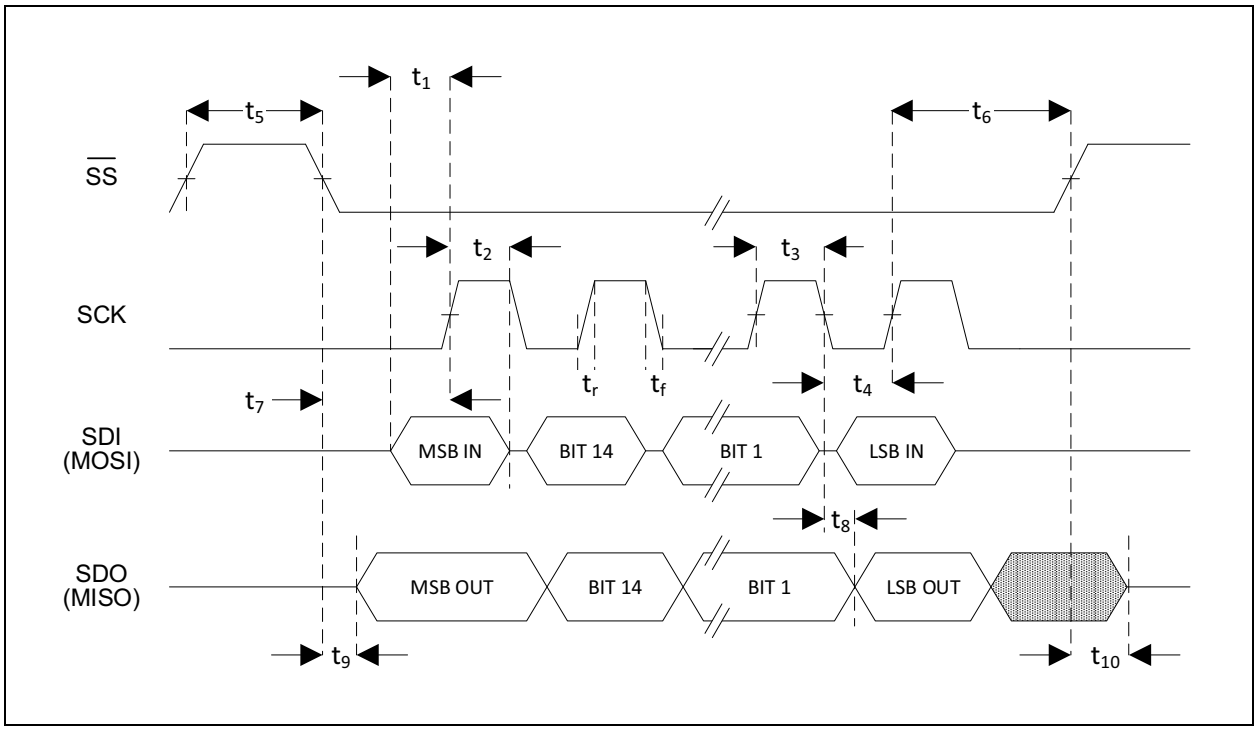


***FIGURE 1-1:*** *SPI Timing Diagram.*


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## HV OPERATIONAL AMPLIFIERS: AC/DC CHARACTERISTICS

Unless otherwise specified, $T_A = T_J = +25°C$. **Boldface** specifications apply over the full operating temperature range $T_A=T_J = 0°C$ to $+125°C$. Typical values are at $+25°C$, $V_{CC} = 6.5V$ unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| HV Op Amps Low Voltage Supply | $V_{CC}$ | 6 | 6.5 | 7 | V | |
| HV Op Amps Low Voltage Supply Current | $I_{CC}$ | — | 0.2 | — | mA | $V_{CC}$ = 6.5V, $V_{PP}$ = 225V, $f_{HVOUT}$ = 124 Hz, sine wave $V_{IN}0,1$= 0 to 2.98V, $C_L$ = 0.22 µF (**Note 1**) |
| HV Op Amps Input Analog Voltage | $V_{IN}0,1$ | 0 | — | 2.98 | V | $V_{PP}$ = 225V, $V_{CC}$= 6.5V |
| High Voltage Supply | $V_{PP}$ | 50 | — | 225 | V | |
| $V_{PP}$ Quiescent Supply Current | $I_{PPQ}$ | — | — | **4.5** | mA | $V_{IN}0,1$= 0V, SHDN = 0 |
| $V_{PP}$ Supply Current | $I_{PP}$ | — | 16.5 | — | mA | $V_{CC}$ = 6.5V, $V_{PP}$ = 225V, $f_{HVOUT}$ = 124 Hz, sine wave $V_{IN}0,1$ = 0 to 2.98V, $C_L$ = 0.22 µF (**Note 1**) |
| $V_{PP}$ Shutdown Supply Current | $I_{PPDN}$ | — | — | 2 | µA | SHDN = 1 |
| $HV_{OUT}$ High Level Output | $V_{OH}$ | 214 | — | — | V | $V_{CC}$ = 6.5V, $V_{PP}$ = 225V, $I_{HVOUT}$ = 100 µA |
| $HV_{OUT}$ Low Level Output | $V_{OL}$ | — | — | 1 | V | $V_{CC}$ = 6.5V, $V_{PP}$ = 225V, $I_{HVOUT}$ = -100 µA |
| HV Op Amps Output Offset Voltage | $HV_{OFFSET}$ | **-1.1** | — | **+1.1** | V | |
| $HV_{OUT}$ Output Source Current | $I_{HVOUT}$ (SOURCE) | 40 | — | — | mA | 100V ≤ $V_{PP}$ ≤ 225V, $V_{CC}$ = 6.5V |
| $HV_{OUT}$ Output Sink Current | $I_{HVOUT}$ (SINK) | 40 | — | — | mA | 100V ≤ $V_{PP}$ ≤ 225V, $V_{CC}$ = 6.5V |
| $HV_{OUT}$ -3 dB Bandwidth | $BW_{124Hz}$ | — | 124 | — | Hz | $V_{PP}$ = 225V, $V_{CC}$ = 6.5V, $C_L$ = 0 to 0.22 µF, $HV_{OUT}$ = Full scale output, 25°C ≤ $T_J$ ≤ 60°C, $R_{BIAS}$ = 150 kΩ (**Note 1**) |
| $HV_{OUT}$ Slew Rate | $SR_{HV}$ | **0.09** | — | — | V/µs | $V_{PP}$ = 225V, $V_{CC}$ = 6.5V, $C_L$ = 0.22 µF |
| Closed Loop Gain | $A_V$ | **72** | **75** | **78** | V/V | $V_{PP}$ = 225V, $V_{CC}$ = 6.5V, No Load |
| Shut Down Input Pin | SHDN | 0.3 | — | 3.3 | V | |
| HV Op Amps Shutdown Time | $t_{SHDN}$ | — | 300 | — | ns | $V_{PP}$ = 225V, $V_{CC}$= 6.5V, SHDN = 0 to 1, $V_{IN}0,1$ = 0 (**Note 2**) |
| HV Op Amps Wake-Up Time from Shutdown | $t_{WKUP}$ | — | 2 | — | ms | $V_{PP}$ = 225V, $V_{CC}$= 6.5V, SHDN = 1 to 0, $V_{IN}0,1$ = 0 (**Note 2**) |
| HV Op Amp Output Preload Capacitor | $C_{PRE}$ | — | 10 | — | nF | **Note 2** |
| **Output Voltage Comparators** | | | | | | |
| Comparator Output High Logic (VOH) | COMP0, COMP1 | 2 | — | 3.3 | V | |
| Comparator Output Low Logic (VOL) | | 0 | — | 0.8 | | |
| Comparator Output Sink Current | $C_{ISINK}$ | — | –2 | — | mA | **Note 1** |
| Comparator Output Source Current | $C_{ISOURCE}$ | — | 2 | — | mA | **Note 1** |
| Comparator Input Offset | $V_{OFFSET}$ | — | 110 | — | mV | **Note 1** |
| Comparator Delay | $t_{DELAY}$ | 0.6 | 1.6 | 2.6 | ms | 1.5 nF at Timer 0, 1 pin, $R_{BIAS}$ = 150 kΩ |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

**2:** Design guidance only.

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## POWER MOSFET: AC/DC CHARACTERISTICS

Unless otherwise specified $T_A = T_J = +25°C$. **Boldface** specifications apply over the full operating temperature range $T_A=T_J = 0°C$ to +125°C. Typical values are at +25°C, EN_CP = 1, $V_{IN}$ = 3.3V, $V_{CC}$ = 6.5V unless otherwise specified.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | BVDSS | 60 | — | — | V | $V_{GS}$ = 0V |
| Drain to Source ON Resistance | $R_{DS}$(ON) | — | — | 10 | mΩ | $V_{GS}$= 5V, ID = 1A (**Note 1**) |
| Diode Forward Voltage | $V_{SD}$ | — | — | 1.2 | V | $I_S$ = 60A, $V_{GS}$ = 0V |

**Note 1:** Design guidance only.

## TEMPERATURE SPECIFICATIONS

**Electrical Characteristics**: Unless otherwise specified, for all specifications $T_A = T_J = +25°C$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperatures Ranges** | | | | | | |
| Operating Junction Temperature | $T_J$ | 0 | — | +125 | °C | |
| Storage Temperature | $T_A$ | –55 | — | +150 | °C | |
| **Package Thermal Resistances** | | | | | | |
| Thermal Resistance (43-Lead VQFN) | $\theta_{JC}$ | — | 1.66 | — | °C/W | **Note 1** |
| | $\theta_{JA}$ | — | 27 | — | °C/W | |

**Note 1:** 4 Layers FR4 4″X4″ PCB.


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## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

### 2.1 DC-to-DC Controller

**Note**: Unless otherwise indicated: $T_A$ = +25°C; Junction Temperature ($T_J$) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

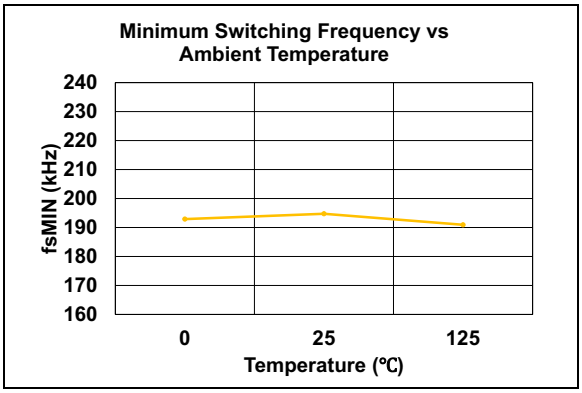


***FIGURE 2-1:*** *Minimum Switching Frequency vs. Ambient Temperature.*

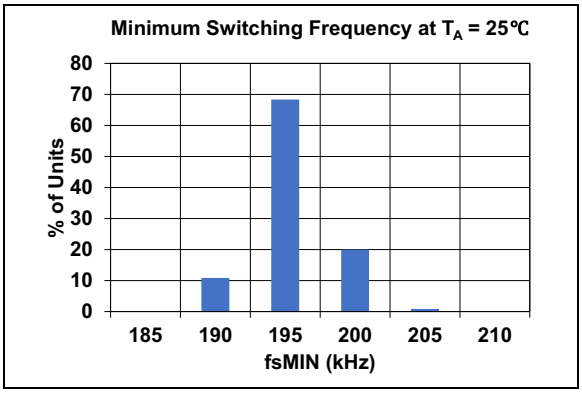


***FIGURE 2-4:*** *Minimum Switching Frequency Distribution at $T_A$ = 25°C.*

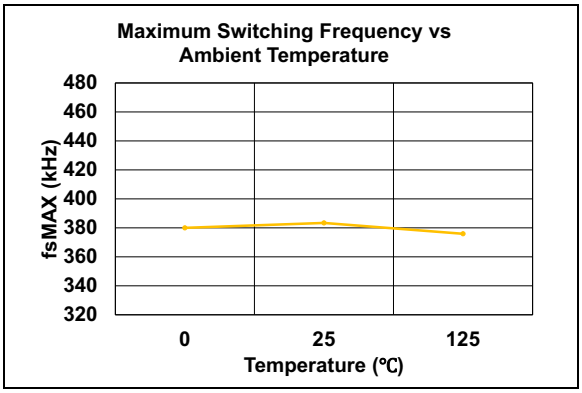


***FIGURE 2-2:*** *Maximum Switching Frequency vs. Ambient Temperature.*

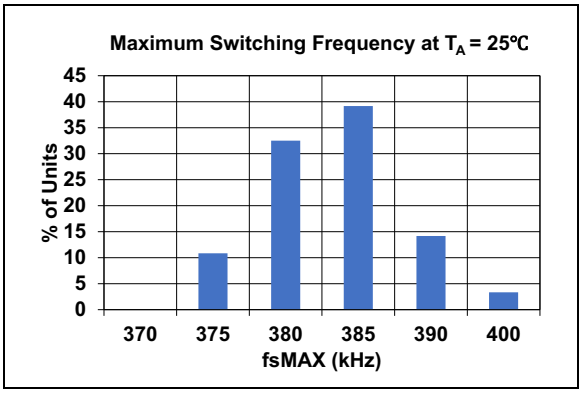


***FIGURE 2-5:*** *Maximum Switching Frequency Distribution at $T_A$ = 25°C.*

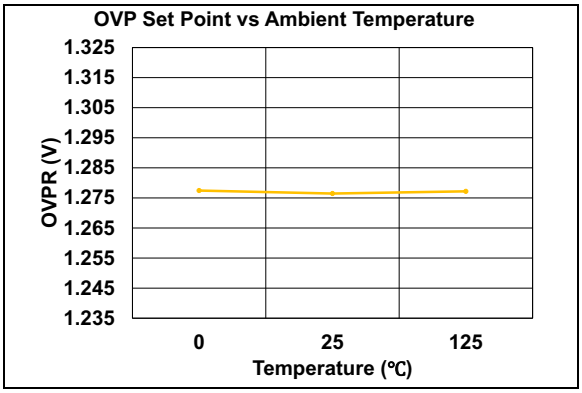


***FIGURE 2-3:*** *OVP Set Point vs Ambient Temperature.*

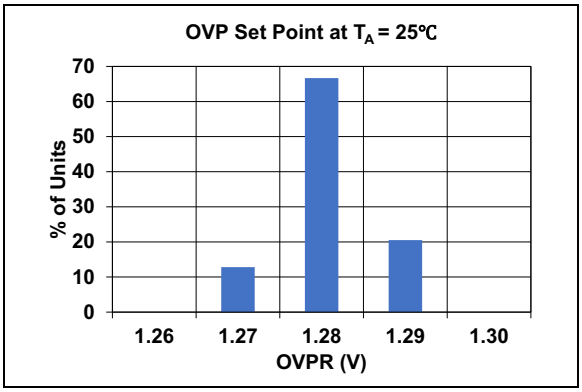


***FIGURE 2-6:*** *OVP Set Point Distribution at $T_A$ = 25°C.*

**Note**: Unless otherwise indicated: $T_A$ = +25°C; Junction Temperature ($T_J$) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

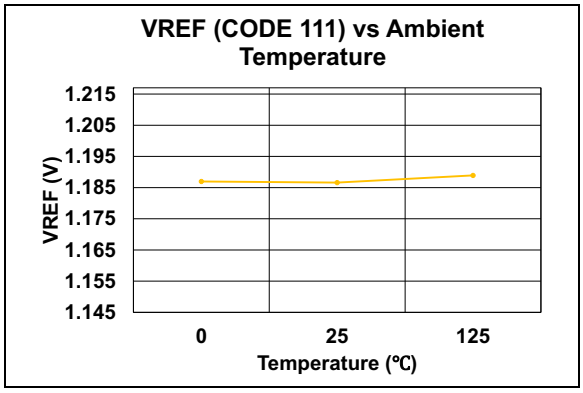


***FIGURE 2-7:*** *VREF (Code 111) vs Ambient Temperature.*

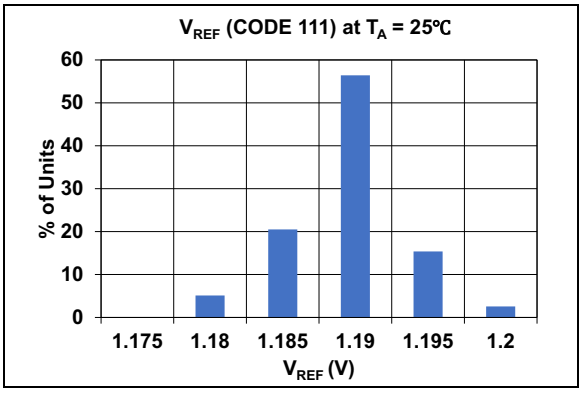


***FIGURE 2-10:*** *VREF (Code 111) Distribution at $T_A$ = 25°C.*

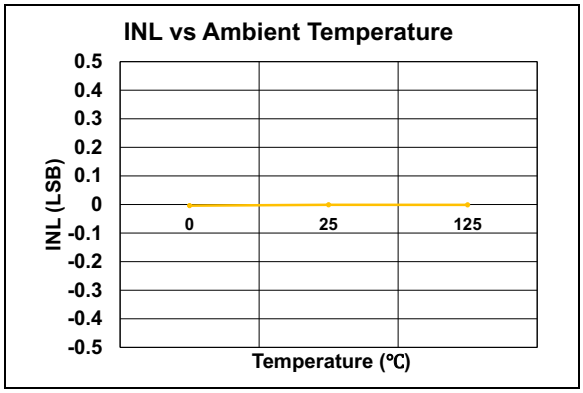


***FIGURE 2-8:*** *INL vs Ambient Temperature.*

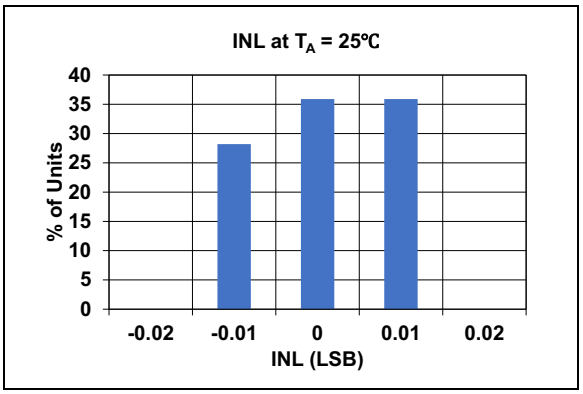


***FIGURE 2-11:*** *INL Distribution at $T_A$ = 25°C.*

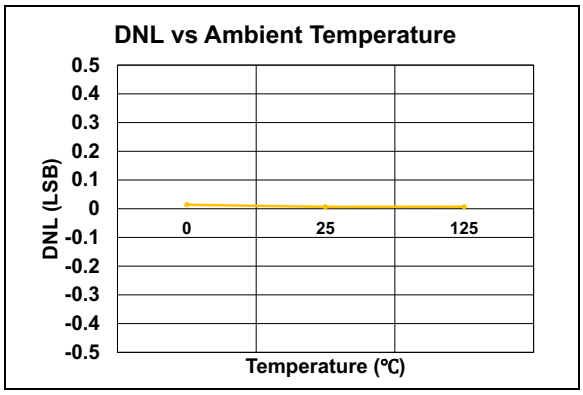


***FIGURE 2-9:*** *DNL vs Ambient Temperature.*

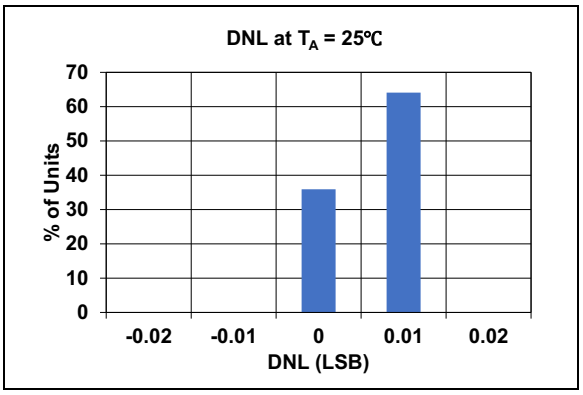


***FIGURE 2-12:*** *DNL Distribution at $T_A$ = 25°C.*


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**Note**: Unless otherwise indicated: $T_A$ = +25°C; Junction Temperature ($T_J$) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

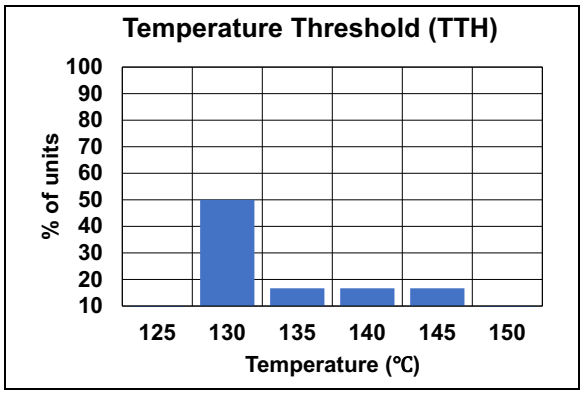


***FIGURE 2-13:*** *Temperature Threshold Distribution.*

## 2.2 HV Amplifiers

**Note:** Unless otherwise indicated: $T_A$ = +25°C; Junction Temperature ($T_J$) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

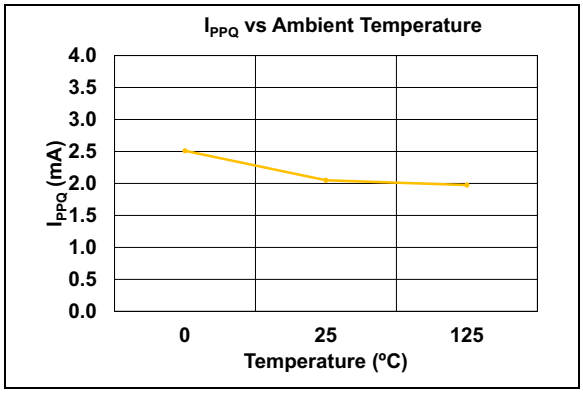


***FIGURE 2-14:*** *$I_{PPQ}$ vs Ambient Temperature.*

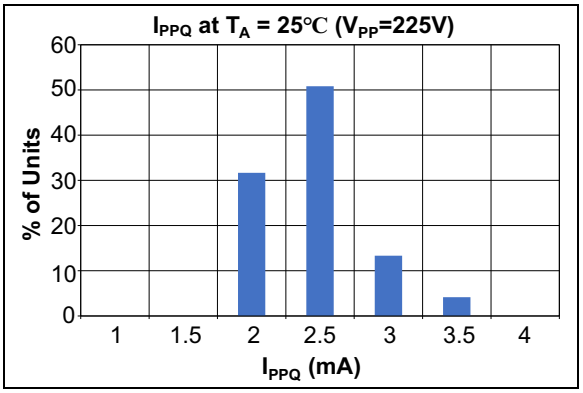


***FIGURE 2-17:*** *$I_{PPQ}$ Distribution at $T_A$ = 25°C.*

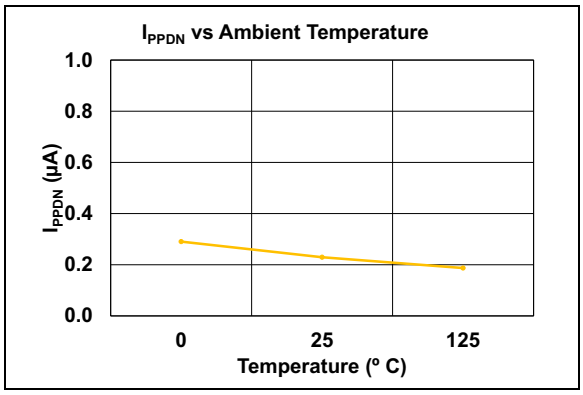


***FIGURE 2-15:*** *$I_{PPDN}$ vs Ambient Temperature.*

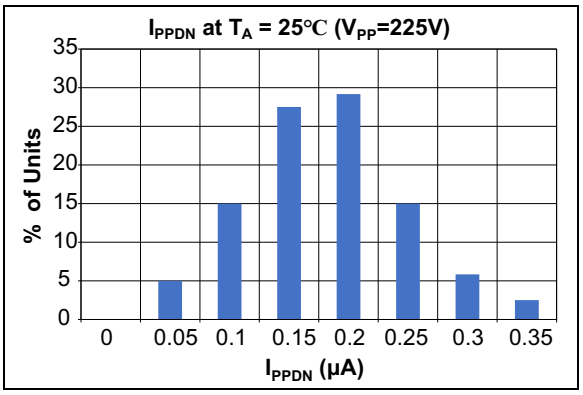


***FIGURE 2-18:*** *$I_{PPDN}$ Distribution at $T_A$ = 25°C.*

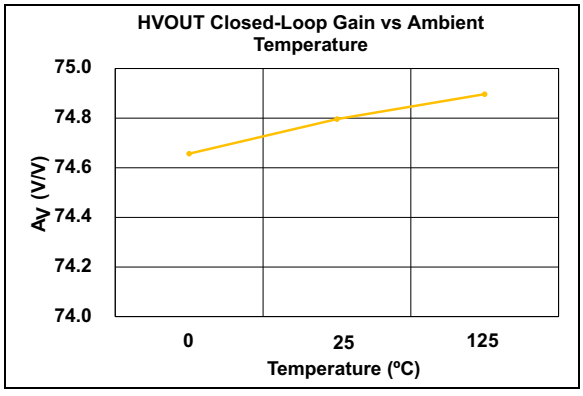


***FIGURE 2-16:*** *HVOUT Closed-Loop Gain vs Ambient Temperature.*

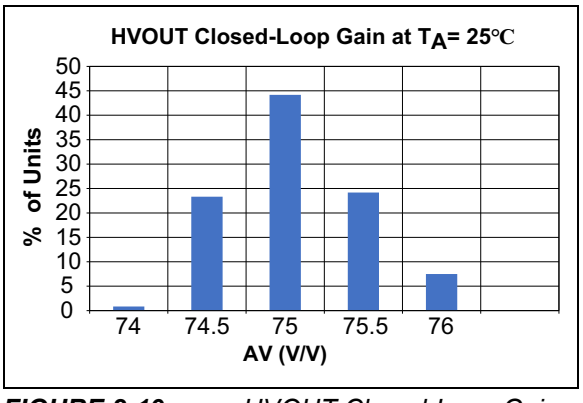


***FIGURE 2-19:*** *HVOUT Closed-Loop Gain Distribution at $T_A$ = 25°C.*


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**Note:** Unless otherwise indicated: $T_A$ = +25°C; Junction Temperature ($T_J$) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

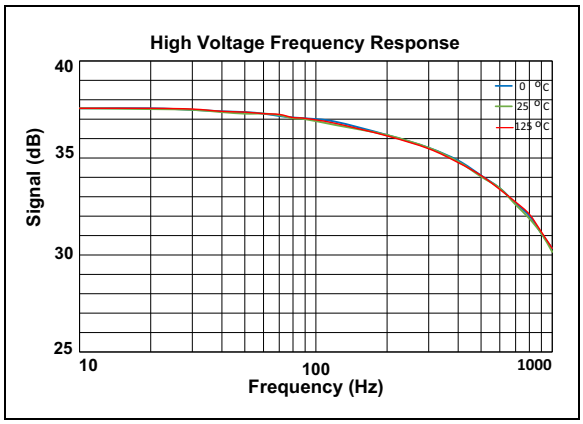


***FIGURE 2-20:*** *High Voltage Frequency Response: Signal vs Frequency ($V_{PP}$ = 225V, $V_{CC}$ = 6.5V, $V_{LL}$ = 3.3V, $R_{BIAS}$ = 150 kΩ, $V_{IN}$ = 0 to 2.98V, Load = 0.22 µF).*

## 2.3 Power MOSFET

**Note:** Unless otherwise indicated: $T_A$ = +25°C; Junction Temperature ($T_J$) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

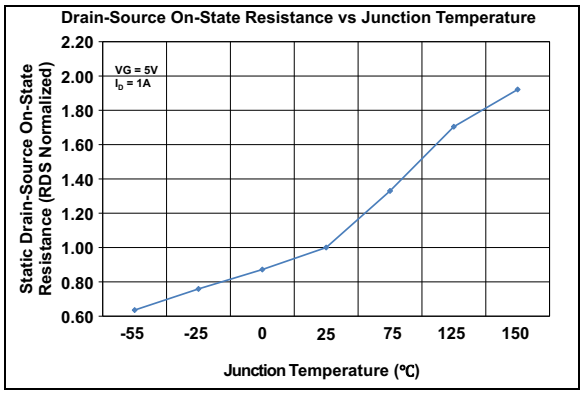


***FIGURE 2-21:*** *Drain-Source On-State Resistance vs Junction Temperature (VG = 5V).*

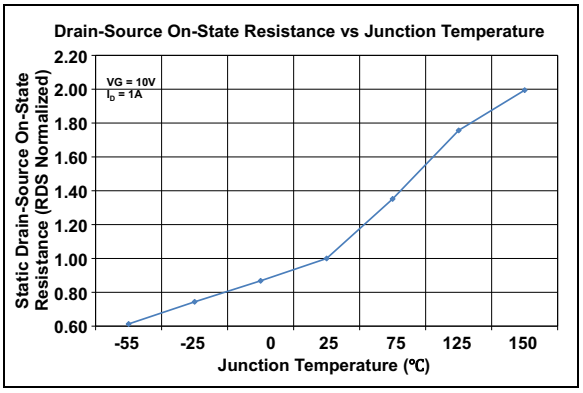


***FIGURE 2-23:*** *Drain-Source On-State Resistance vs Junction Temperature (VG = 10V).*

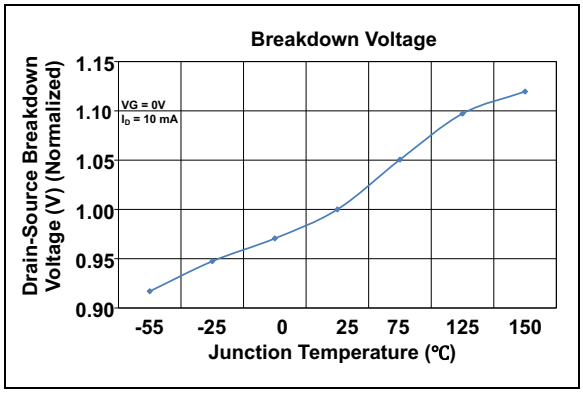


***FIGURE 2-22:*** *Breakdown Voltage.*

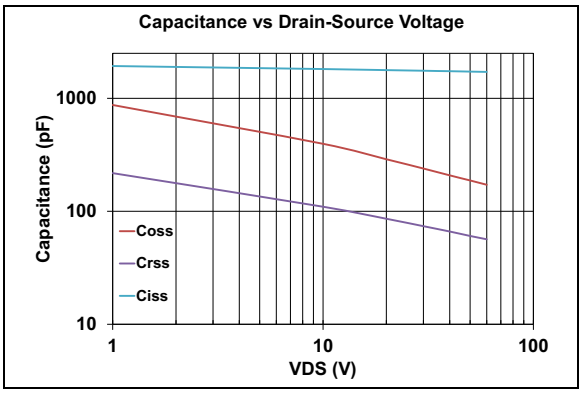


***FIGURE 2-24:*** *Capacitance vs Drain-Source Voltage.*


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## 3.0 PACKAGE PIN CONFIGURATION AND FUNCTION DESCRIPTION

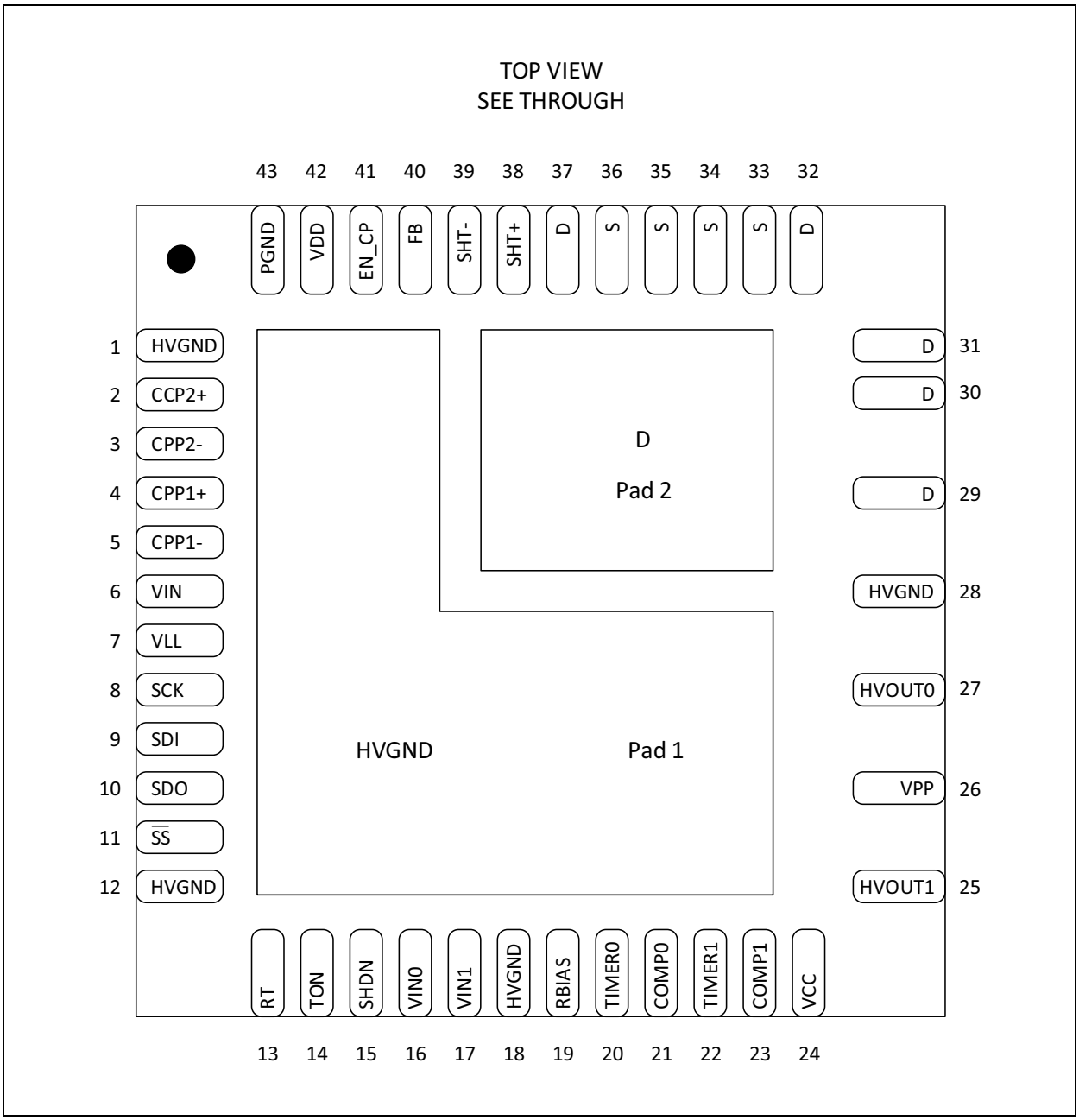


***FIGURE 3-1:*** *VQFN 43-Lead 7 x 7 mm.*

## 3.1 Pin Description

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| PIN | Symbol | Description |
|---|---|---|
| 1 | HVGND | High Voltage Ground |
| 2 | CCP2+ | Charge Pump Storage Capacitor #2 Plus Terminal |
| 3 | CCP2- | Charge Pump Storage Capacitor #2 Minus Terminal |
| 4 | CCP1+ | Charge Pump Storage Capacitor #1 Plus Terminal |
| 5 | CCP1- | Charge Pump Storage Capacitor #1 Minus Terminal |
| 6 | $V_{IN}$ | Input Voltage Supply |
| 7 | $V_{LL}$ | Logic Output Voltage Supply |
| 8 | SCK | SPI Clock |
| 9 | SDI | SPI Data Input |
| 10 | SDO | SPI Data Output |
| 11 | $\overline{SS}$ | SPI Chip Select |
| 12 | HVGND | High Voltage Ground |
| 13 | RT | Frequency Adjustment Pin for DC-to-DC Controller |
| 14 | TON | TON Timer for Pulse Width Modulation |
| 15 | SHDN | Shutdown Output Pin |
| 16 | $V_{IN}0$ | CH0 Amplifier Input |
| 17 | $V_{IN}1$ | CH1 Amplifier Input |
| 18 | HVGND | High Voltage Ground |
| 19 | $R_{BIAS}$ | Bias Reference for High Voltage Amplifiers |
| 20 | Timer0 | Delay Timer 0 |
| 21 | Comp0 | Comparator Output 0 |
| 22 | Timer1 | Delay Timer 1 |
| 23 | Comp1 | Comparator Output 1 |
| 24 | $V_{CC}$ | Low Voltage Amplifier Supply |
| 25 | $HV_{OUT}1$ | CH1 High Voltage Amplifier Output |
| 26 | $V_{PP}$ | High Voltage Amplifier Supply |
| 27 | $HV_{OUT}0$ | CH0 High Voltage Amplifier Output |
| 28 | HVGND | High Voltage Ground |
| 29,30,31,32,37, Pad 2 | D | Power MOSFET Drain |
| 33,34,35,36 | S | Power MOSFET Source |
| 38 | SHT+ | Current Sense + Terminal |
| 39 | SHT- | Current Sense - Terminal |
| 40 | FB | Power Supply Feedback Input |
| 41 | EN_CP | Charge Pump Enable Input Pin |
| 42 | $V_{DD}$ | Charge Pump Output Voltage |
| 43 | PGND | Power Ground |


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### 3.2 Charge Pump Storage Capacitors (CPP2+, CPP2-, CPP1+, CPP1-)

The storage capacitors input pins are used for the internal charge pump to generate **$V_{DD}$.** $V_{DD}$ is the required voltage source to operate all the circuitry in the DC-to-DC Controller and the HV Op Amps bias currents, $V_{CC}$. 2 µF capacitors are recommended for both storage capacitors, CPP1 and CPP2.

### 3.3 Input Voltage Supply ($V_{IN}$)

Input Voltage Supply pin for internal circuitry of the device and for the non-isolated flyback configuration. The device is intended for battery operated applications with a voltage range of 2.7V to 5.5V.

### 3.4 Logic Voltage Supply Output Pin ($V_{LL}$)

$V_{LL}$ is an internally generated 3.3V voltage source for the SPI interface. $V_{LL}$ is an output pin and can be used to power the other family device, HV56022, that requires a 3.3V voltage source. A 1 µF bypass capacitor is recommended to be connected at the $V_{LL}$ output pin.

### 3.5 SPI- Serial Clock (SCK)

Serial clock pin for the SPI interface.

### 3.6 SPI- Serial Data Input (SDI)

Serial data input pin for the SPI interface.

### 3.7 SPI- Serial Data Output (SDO)

Serial data output pin for the SPI interface.

### 3.8 SPI- Serial Chip Select ($\overline{SS}$)

Serial data chip select pin for the SPI interface.

### 3.9 High Voltage Ground (HVGND)

Ground reference pins for the High Voltage Amplifiers.

### 3.10 Power Ground (PGND)

Ground reference pin for the DC-to-DC converter, the internal Power MOSFET, and the short circuit sense resistor, $R_{SHT}$. The power ground separates the

DC-to-DC converter switching noise from the rest of the circuitry.

### 3.11 Frequency Adjustment (RT)

Adjustment input pin for the DC-to-DC converter PWM switching frequency, fs. A 200 kΩ resistor will set the switching frequency to 400 kHz (typical).

fs = 1/((RT*12 pF)+100 ns)

### 3.12 Duty Cycle On Time (TON)

The On-Time input pin takes a voltage reference, VTON, to set the PWM (Pulse Width Modulation) duty cycle. TON voltage range is from $0.25V_{TS}$ to $0.8V_{TS}$ to generate a 25% to 80% duty cycle, respectively.

### 3.13 Shutdown Output Pin (SHDN)

The Shutdown output pin is used to deactivate the other family device, HV56022 Dual High Voltage Amplifiers, when both devices are used in the same application. The HV Op Amps shutdown option is available at the RXB Register over the SPI interface; see **Section 4.2.13 "SPI Control Registers"** for more details.

### 3.14 High Voltage Amplifiers Inputs ($V_{IN}0$, $V_{IN}1$)

Input data signals for the High Voltage Operational Amplifiers.

### 3.15 Amplifiers Bias Reference Pin ($R_{BIAS}$)

High Voltage Amplifiers bias reference input pin. A 150 kΩ resistor will set the bias currents for a 124 Hz, –3 dB bandwidth for 225V sinusoidal waveforms driving 0.22 µF capacitive loads.

### 3.16 Output Voltage Comparator Output Pins (COMP0, COMP1)

The internal voltage comparators monitor the input data signals, $V_{IN}0$,$V_{IN}1$, and the High Voltage Amplifiers' feedback signals for a short at the amplifiers' outputs. The comparators monitor for a 20% or greater voltage drop in the output against the input signal before reporting a short flag, COMP0,1 = 1 or 3.3V.

### 3.17 Output Voltage Comparators Delay Timer Pins (Timer0, Timer1)

The output voltage comparators monitor the input data signals, $V_{IN}0$, $V_{IN}1$, against the HV Op Amp feedback signals: if there is a heavy capacitive load, the HVOUT signals will slowly increase, causing the comparators to detect a false short. False triggering is avoided by adding a delay to the input signals of the comparators. A 1.5 nF capacitor will add a 1.6 ms delay time when $R_{BIAS}$ is set to 150 kΩ.

**Time Delay** = 7.55*$R_{BIAS}$*C (Timer)

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### 3.18 Low Voltage Supply Input Pin for High Voltage Amplifiers ($V_{CC}$)

$V_{CC}$ is the low voltage supply input pin for the High Voltage Op Amps and has an operational voltage range of 6V to 7V. $V_{CC}$ is intended to be biased from the internal charge pump converter output voltage, $V_{DD}$. A 2 µF bypass capacitor is recommended to be added close to the $V_{CC}$ pin.

### 3.19 High Voltage Amplifiers Outputs ($HV_{OUT}0$, $HV_{OUT}1$)

High Voltage Amplifiers Output channels.

### 3.20 High Voltage Amplifiers Supply Input Pin ($V_{PP}$)

Input power supply pin for the High Voltage Op Amps. $V_{PP}$ is generated by the flyback configuration formed by the internal power MOSFET, the DC-to-DC Controller, and the external transformer. The maximum operating voltage is 225V. A 0.1 µF or higher bypass capacitor is recommended to be added close to the $V_{PP}$ pin.

### 3.21 Power MOSFET Drain (D)

Drain pin connections for the internal Power MOSFET.

### 3.22 Power MOSFET Source (S)

Source pin connections for the internal Power MOSFET.

### 3.23 Current Sense Resistor Input Pins (SHT-, SHT+)

Current sense resistor input pins for the Short Circuit Protection circuitry in the DC-to-DC Controller.

### 3.24 Power Supply Feedback Input Pin (FB)

Feedback input pin for the DC-to-DC Controller.

### 3.25 Charge Pump Enable Input Pin (EN_CP)

Internal Charge Pump enable control pin.

EN_CP = '1' or 3.3V enables $V_{DD}$; EN_CP = '0' or 0.V disables $V_{DD}$.

### 3.26 Charge Pump Output Voltage ($V_{DD}$)

Charge pump output voltage source for the DC-to-DC internal circuitry and $V_{CC}$. $V_{DD}$ is designed to supply voltage source for the HV56020 as well as for the HV56022, which is part of the same device family. A 10 µF or greater capacitor is recommended for decoupling.


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## 4.0 FUNCTIONAL DESCRIPTION

The HV56020 is a Multi-Chip Module (MCM) driver solution designed for Haptic Applications. The IC consists of three devices: (1) Dual High Voltage Operational Amplifiers, (2) a DC-to-DC Converter Controller, and (3) a Power MOSFET.

The High Voltage Operational Amplifiers operate up to 225V and can source/sink 40 mA minimum peak currents. The amplifiers are designed for a –3 dB bandwidth of 124 Hz for 225V sinusoidal waveforms driving 0.22 µF capacitive loads. In addition, the amplifiers are paired with output voltage comparators to monitor and report short circuit conditions.

The DC-to-DC Controller and the power MOSFET along with an external transformer generate the required voltage supply for the High Voltage Op Amps using a Non-Isolated Flyback configuration. The DC-to-DC Controller also includes many protection circuitries: Over and Undervoltage Protection, Short Circuit Protection (DC-to-DC), Power ON Reset, and a Temperature Sensor.

The power MOSFET is a 60V device with a 10 mΩ On resistance and a 14 nC gate charge. The MOSFET allows the flyback configuration to sustain a 400 kHz switching frequency.

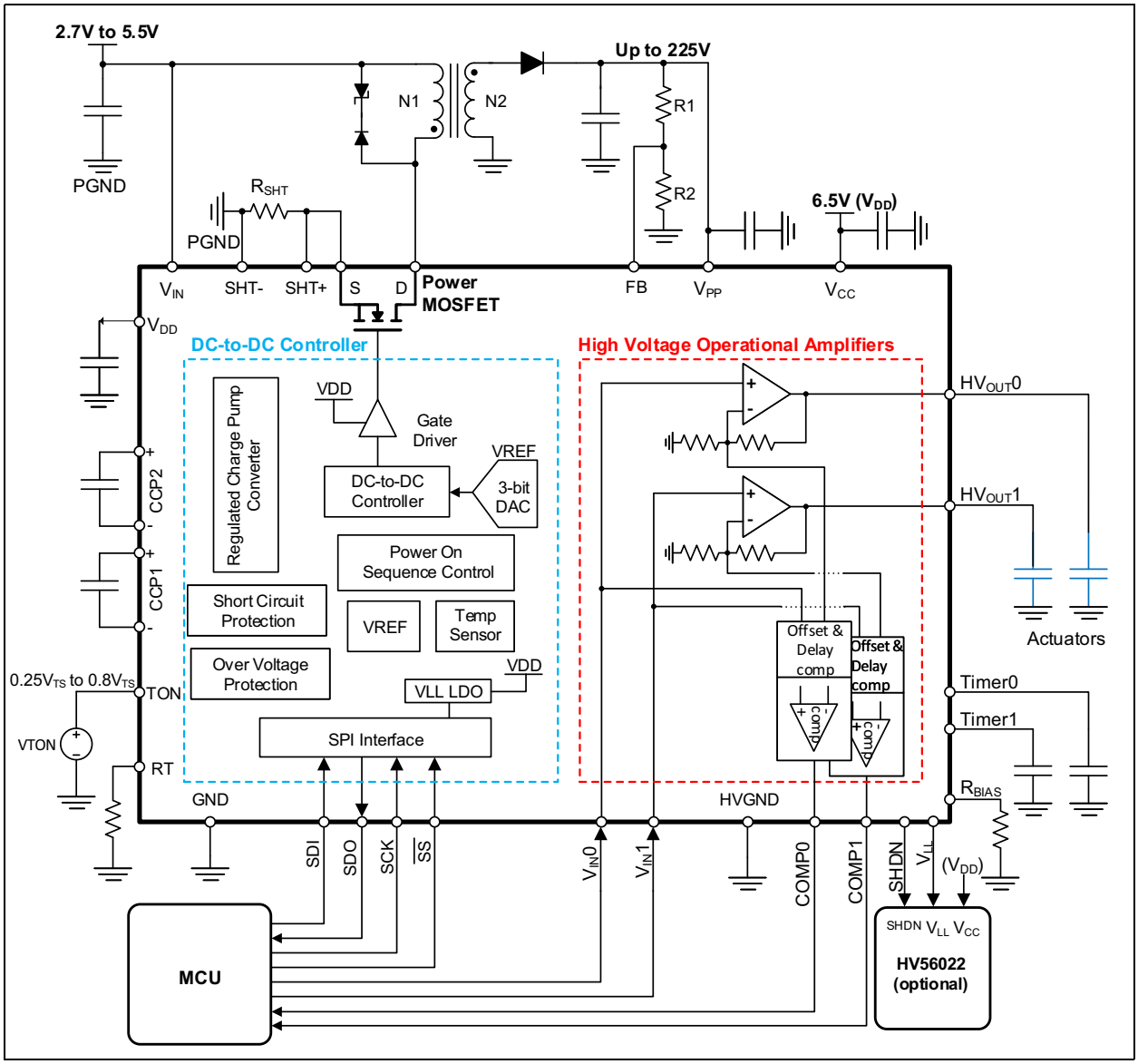


***FIGURE 4-1:*** *Functional Block Diagram.*

## 4.1 High Voltage Operation Amplifiers

The High Voltage Operational Amplifiers operate up to 225V (unipolar) with 40 mA minimum source/sink peak current capabilities and are designed with a fixed 75V/V gain.

### 4.1.1 BANDWIDTH

The amplifiers' bandwidth is controlled in part by the internal bias currents set by an external resistor, **$R_{BIAS}$**. The internal bias currents can be increased by reducing $R_{BIAS}$ to achieve higher Bandwidth. Increasing the Bandwidth will lead to higher power consumption. A 150 kΩ $R_{BIAS}$ will set the bias currents for a 124 Hz,

–3 dB, Bandwidth for 225V sinusoidal waveforms driving 0.22 µF capacitive loads.

### 4.1.2 STABILITY

Amplifiers are designed to operate for a wide range of capacitive loads and to maintain stability when light or no loads are present. 10 nF preload capacitors, **$C_{PRE}$**, are recommended to be added in parallel with the outputs **$HV_{OUT}0$** and **$HV_{OUT}1$**. Figure 4-2 illustrates the application diagram using 10 nF preload capacitors.

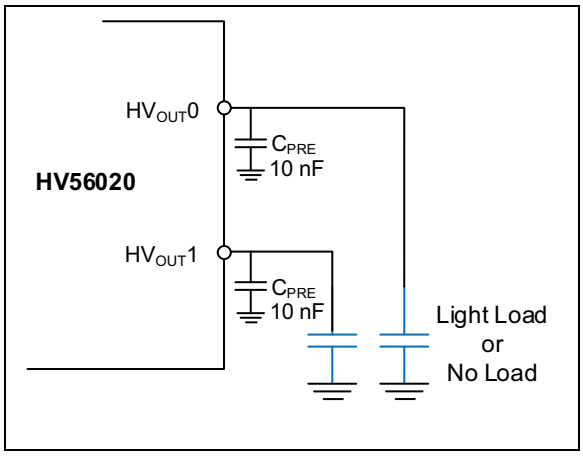


***FIGURE 4-2:*** *Preload Capacitors.*

### 4.1.3 SHORT CIRCUIT DETECTION

Amplifiers are paired with voltage comparators for output short circuit detection. The Output Voltage Comparators, **COMP0** and **COMP1,** are a safety feature designed to check the voltage across the load (haptic actuator) during operation. Comparators monitor the Amplifiers' feedback signals against 80% of the input signals, **$V_{IN}0$** and **$V_{IN}1$**. If there is a short or failing load (drooping voltage) at the output, a flag ('1' or 3.3V) will be raised by the comparators for the MCU (controlling host).

Comparators are designed with internal voltage offset, **$V_{OFFSET}$** (~110 mV) and delay timer pins, **Timer0** and **Timer1**, to prevent false triggering.

The internal voltage offsets are designed to avoid false triggering due to ground noise when input signals swing close to zero level.

Timer pins add delay compensation to the comparators' inputs, **$V_{IN}0$** and **$V_{IN}1$**, by using capacitors at the Timer0 and Timer1 pins. When input signals are step functions (for example square waves), the amplifiers' outputs will slowly charge, producing trapezoidal waveforms. If input signals are not delayed, amplifiers' feedback signals will appear as short when compared to the input signals. A 150 kΩ $R_{BIAS}$ and timer pins with 1.5 nF capacitors will provide a 1.6 ms delay. Figure 4-3 illustrates a false detection event when timer capacitors are not being used.

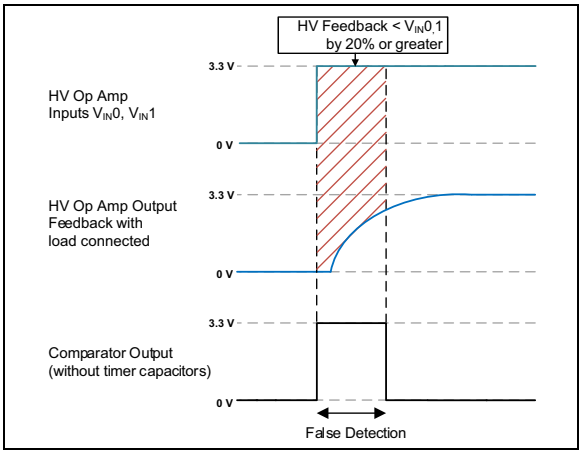


***FIGURE 4-3:*** *False Detection.*

### 4.1.4 SHUTDOWN MODE

The shutdown mode, **SHDN,** disables the internal bias current, allowing for power saving when the amplifiers are not operating. The shutdown mode is available in the RXB Register Bit 1, **SHDN**; see **Section 4.2.13 "SPI Control Registers"** for more details.


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## 4.2 DC-to-DC Controller

A Hysteretic Step-up DC-to-DC Controller is integrated in this driver IC to generate the high voltage rail, $V_{PP}$, required to power the High Voltage Amplifiers. The feedback input is a typical DC-to-DC feedback which monitors the feedback voltage from a resistor divider referenced to ground. When the sensing voltage is higher than the internal reference voltage, $V_{REF}$, it deactivates the pulse in the next cycle. When the sensing voltage is lower, it activates the pulse.

The DC-to-DC controller consists of a Charge Pump Regulator, PWM Controller, Oscillator Circuit, 3-Bit DAC for Voltage Reference, Overvoltage Protection, Short Circuit Protection, Temperature Sensor, Power-On Reset and a 16-bit Serial Peripheral Interface (SPI).

### 4.2.1 CHARGE PUMP REGULATOR

The internal charge pump regulator runs at a fixed switching frequency to generate **$V_{DD}$**, a 6.5V voltage source with 15 mA supply current. $V_{DD}$ is the voltage source required to drive the gate of the internal power MOSFET, the DC-to-DC circuitry, and the High Voltage Amplifiers bias currents, **$V_{CC}$**. The enable charge pump input pin, **EN_CP**, turns ON the charge pump when it is High, and OFF when it is pulled Low or Open. $V_{DD}$ is also designed to provide power for additional HV56022 devices ($V_{CC}$).

### 4.2.2 POWER-ON-RESET

The Power-on-Reset circuit ensures $V_{DD}$ voltage has reached the operational mode, **$VDD_{UVLO}$**, (4.5V typical) before the internal circuitry is turned ON. The Power-on-Reset circuit also prevents the internal circuitry from running in case $V_{DD}$ voltage drops below the non-operational mode, $VDD_{UVLO}$ - **$VDD_{HYST}$**.

### 4.2.3 CLOCK GENERATION

The internal clock source is generated by an internal bias current set by an external resistor, **RT**. The frequency adjustment pin, RT, recommended range is from 200 kΩ to 400 kΩ to generate a 400 kHz to 200 kHz clock source respectively.

fs = 1/((RT*12pF)+100ns)

### 4.2.4 GATE DRIVER

The gate driver is designed to drive the internal power MOSFET transistor to the maximum switching frequency **$f_{s,MAX}$**. The gate driver swings between $V_{DD}$ and ground to drive the power MOSFET with fast rise and fall transition times.

### 4.2.5 VOLTAGE REFERENCE

The voltage reference sets the DC-to-DC output voltage, **$V_{PP}$**, when the IC is configured in a flyback configuration (suggested topology). The voltage reference, **$V_{REF}$**, is specified by a 3-Bit code word and is set over the 16-Bit SPI interface (see **Section 4.2.12 "SPI Serial Interface Mode 0"** for more details). The 3-Bit code word allows for 8 different voltage levels starting with 000 equivalent to 67.5V, and 111 equivalent to 225V. Table 4-1 shows the complete operational values. The code word setting corresponds to a percentage of the $V_{REF}$ that is set to be **1.188V.** The minimum setting is 000, which corresponds to 30% of $V_{REF}$, and 111 to 100%. The maximum recommended operating $V_{PP}$ voltage is 225V. To set $V_{PP}$ to zero, the device needs to be disabled by the **EN** Bit (EN = '0') or set in a standby mode by **STD_BY** Bit **(STD_BY = '1', EN = '1')**.

**TABLE 4-1: 3-BIT DAC TO OUTPUT VOLTAGE**

| DAC <7:5> | $V_{REF}$ (%) | $V_{PP}$ (V) |
|---|---|---|
| 000 | 30 | 67.5 |
| 001 | 40 | 90 |
| 010 | 50 | 112.5 |
| 011 | 60 | 135 |
| 100 | 70 | 157.5 |
| 101 | 80 | 180 |
| 110 | 90 | 202.5 |
| 111 | 100 | 225 |

### 4.2.6 OVERVOLTAGE PROTECTION

The Overvoltage Protection ($OVP_R$) circuitry monitors the DC-to-DC Controller output voltage, $V_{PP}$, for an overvoltage condition by checking the feedback voltage, VFB. If the output voltage surpasses 8% of maximum $V_{PP}$ (225V), the Overvoltage protection circuitry will shut down the DC-to-DC Controller to prevent damage to the IC. In case of an Overvoltage condition there will also be an Overvoltage flag, OVER, reported in the TXB Register.

### 4.2.7 SHORT CIRCUIT PROTECTION

A short circuit at the output of the flyback transformer may cause damage to the power supply circuit and to the application system. A short circuit protection scheme is implemented in the DC-to-DC controller by monitoring the power MOSFET Source-to-Ground current with a sense resistor, **$R_{SHT}$**. Short circuit is indirectly detected by sensing the inductor's saturation.

The presence of a higher than designed current through $R_{SHT}$ will cause the voltage drop across the sense resistor to be greater than the 50 mV threshold offset voltage, **$SH_{OFF}$**, causing the short circuit condition, suspending DC-to-DC operation, and raising a **SHORT** flag in the TXB Register. The short circuit protection circuit can be enabled or disabled by the **SHT_EN** Bit in the RXB Register.

### 4.2.8 STANDBY MODE (STD_BY)

The standby mode sets the HV56020 into power saving mode when there are no actuations required at the High Voltage Outputs (HVOUTs), by disabling the DC-to-DC converter output, $V_{PP}$. The standby bit, **STD_BY**, is available at the RXB Register Bit 3. The standby mode stops PWM pulses for power MOSFET and keeps the rest of the device running until the full operational mode is enabled, EN = '1' and STD_BY = '0'.

### 4.2.9 ENABLE CONTROL (EN)

Enable control input bit, **EN**, for the DC-to-DC Controller is available in the RXB Register Bit 2. In disabled mode, EN = '0', all internal circuitry except the wake-up circuit is turned off. The wake-up circuit restores the internal circuitry to normal operation when the enable bit is set high, EN = '1'.

### 4.2.10 TEMPERATURE SENSOR

The Temperature Sensor helps to ensure that the maximum operational temperature of the IC, +150°C, is not exceeded. If the temperature of the device reaches the threshold temperature range, $\mathbf{T_{TH}}$, the **TEMP** flag Bit will be set to '1' in the TXB Register. The Temperature Sensor has a +25°C hysteresis that resets the TEMP Bit flags to '0' once temperature drops below the hysteresis threshold temperature, $\mathbf{T_{THHYST}}$. The Temperature Sensor is only an indicator and will NOT perform any further action to the DC-to-DC or HV Op Amps.

### 4.2.11 TON GENERATION

TON input pin takes a voltage reference to set the duty cycle, **TON**, of the Pulse Width Modulation (PWM) cycles for the internal gate driver. The voltage range is $0.25V_{TS}$ to $0.8V_{TS}$ to generate 25% to 80% duty cycle respectively, where $\mathbf{V_{TS}}$ is typically 3.5V.

To have a soft start-up, low input peak currents, in the flyback topology it is recommended to start increasing the PWM duty cycle slowly until the topology has reached the designed PWM duty cycle, TON. The slow increase in the TON is achieved by slowly increasing the **VTON** voltage reference. The diagram in Figure 4-4 shows two cases: when no soft start-up and when soft start-up is implemented using VTON. A 10 ms time constant is recommended for soft start-up.

Toggling EN or STBY Bit will reset the internal, VTON, voltage reference for PWM duty cycle. A TON reset ensures a soft start-up mode when EN or STBY are used multiple times during operation.

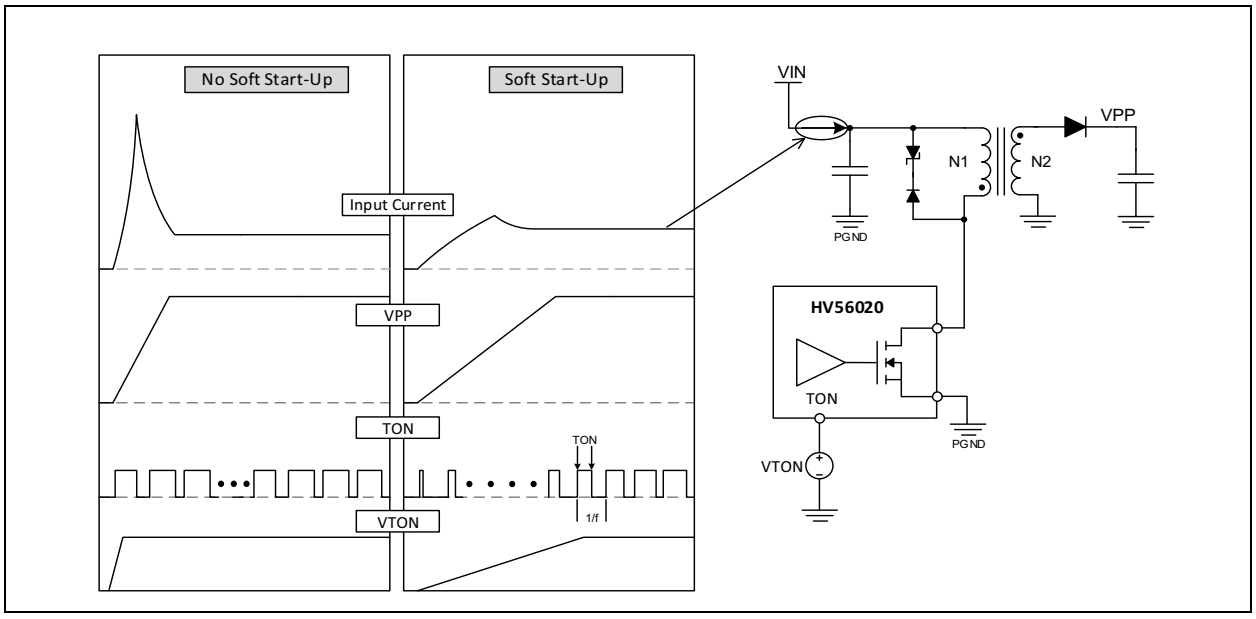


***FIGURE 4-4:*** *TON Soft Start-Up Implementation.*


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### 4.2.12 SPI SERIAL INTERFACE MODE 0

The HV56020 uses a 16-bit Serial Peripheral Interface (SPI) module to communicate with the host controller. The serial synchronous interface is used to control and monitor the DC-to-DC Step-Up converter. The SPI module is designed to be compatible with operation Mode 0.

In Mode 0, data transmission starts when $\overline{SS}$ goes Low, causing the Slave to output the Most Significant Bit (MSB) data in to the SDO (MISO) pin. Data transfer between Master and Slave takes place during the rising edge of the clock (SCK), which is considered to be idle when it is Low. This mode of operation requires data for Master and Slave to be present in the line (MISO/MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data are pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first transaction, 16-Bit data exchange, Master writes the latest data (Dn) to Slave, while Slave passes its previous (Dn-1) stored data to the Master. Figure 4-5 illustrates the 16-bit operation mode.

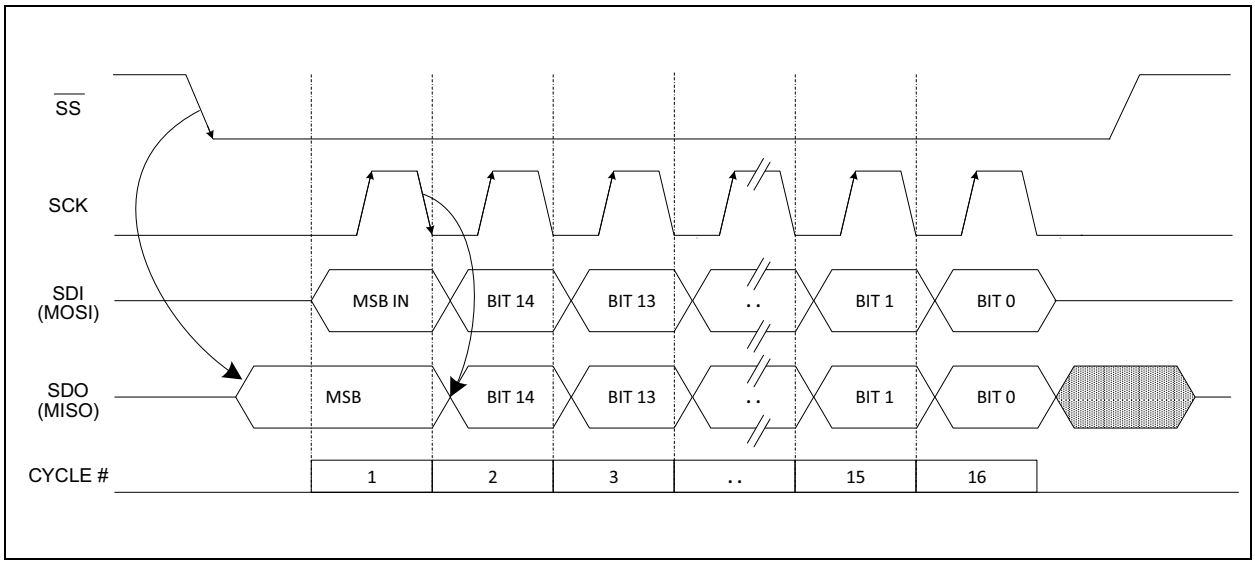


***FIGURE 4-5:*** *16-Bit SPI Mode 0.*

### 4.2.13 SPI CONTROL REGISTERS

The 16-Bit SPI Interface module consists of two 8-Bit registers, a Receive Register, RXB, and a Transmit Register, TXB.

The Receive Register (**RXB**) is where the control settings for the DC-to-DC Controller are specified, for example, the Step-Up voltage level ($V_{PP}$), Short Circuit Detection Enable (SHT_EN), Standby (STD_BY), Enable (EN) and Shutdown (SHDN) modes of operation.

The Transmit Register (**TXB**) is used by the DC-to-DC converter to report the current operation state by using various status flags like Overtemperature (TEMP), Short Circuit (SHORT), Overvoltage Detection (OVER) at $V_{PP}$, and whether the Step-Up voltage ($V_{PP}$) is ready for operation (READY).

To operate the DC-to-DC controller, only 8 bits of data are required, and correspond to the lower byte. The upper byte is a place holder used by the TXB register to report the status of the DC-to-DC controller, see Figure 4-6. The Most Significant Bit (MSB) of data is written (to SDI/MOSI pin) and read (pushed out of SDO/MISO pin) first.

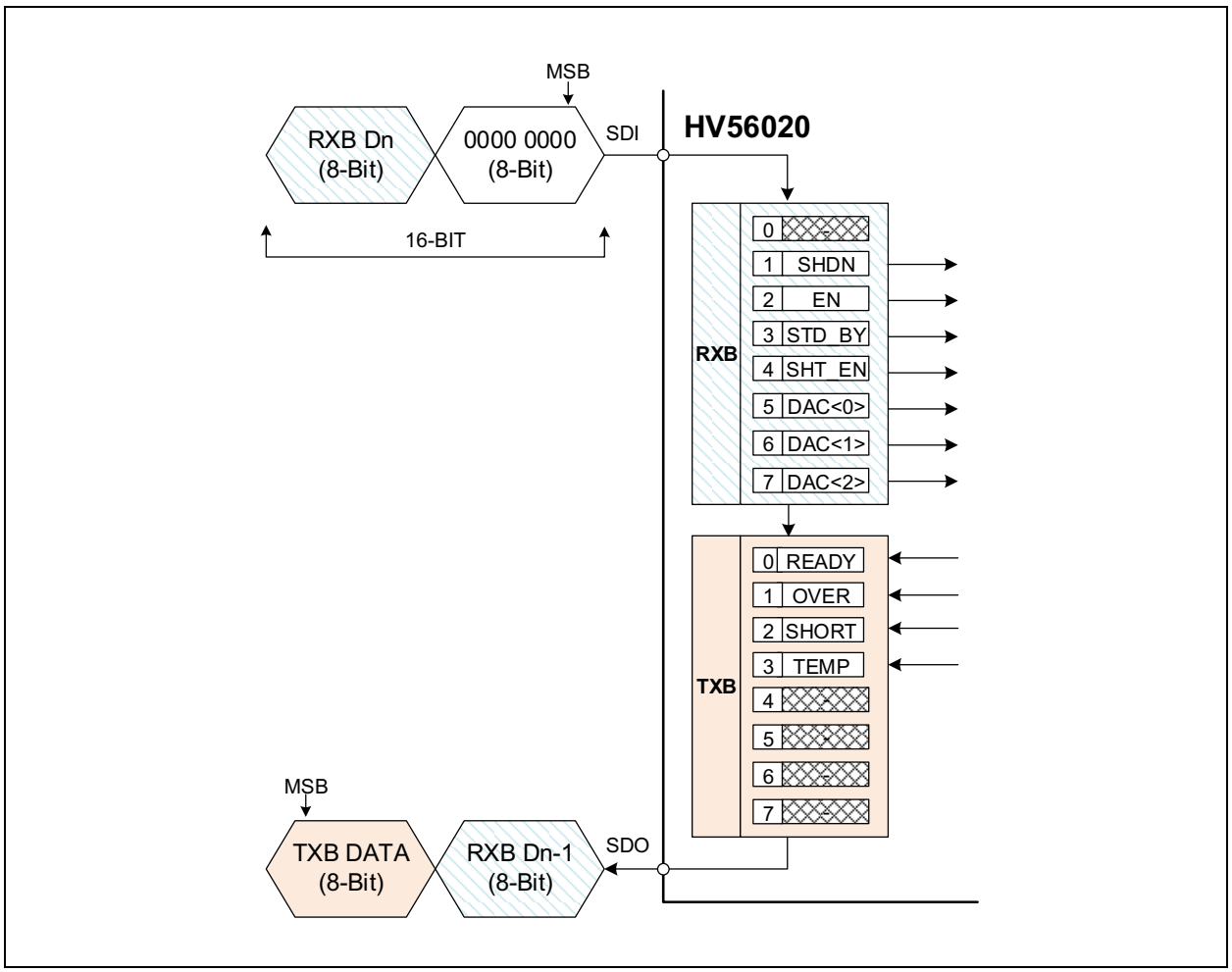


***FIGURE 4-6:*** *SPI Registers: RXB, TXB.*


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### 4.2.13.1 RECEIVE REGISTER (RXB)

**TABLE 4-2: RECEIVE REGISTER (RXB)**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | U-0 |
|---|---|---|---|---|---|---|---|
| DAC<2:0> | | | SHT_EN | STD_BY | EN | SHDN | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **DAC[2:0]:** VREF 3-Bit Code Word

Bits **DAC[7:5]** set the DC-to-DC output voltage, $V_{PP}$. Table 4-3 presents the corresponding code word values for the desired $V_{PP}$ voltage.

bit 4 **SHT_EN:** Short Circuit Protection Enable

1 = Enables the detection of short circuit when the DC-to-DC is operating. In case of a short (high current event on Power-FET; SHT+ and SHT-) the SHORT Flag will be raised and reported on the TXB Register Bit 2 and DC-to-DC will suspend operation.

0 = Disables the detection of short circuit events, and not SHORT Flag is reported in the TXB Register. This feature is typically used during the initial start up of the Step-Up converter (Flyback) where it will be operating in a CCM mode momentarily (high current on SHT+ and SHT- pins) to avoid false flags on TXB Register Bit 2.

Note**:** if SHT_EN = 0, state of SHORT = 0.

bit 3 **STD_BY:** Standby Mode

1 = Disables the DC-to-DC converter output voltage, the rest of the circuitry keeps running.
0 = Standby mode disabled.

bit 2 **EN:** DC-to-DC Step-Up Converter Enable

1 = DC-to-DC enabled.
0 = DC-to-DC disabled.

bit 1 **SHDN:** High Voltage Amplifiers Shut Down

1 = Disables the HV Op amps.

0 = Enables the HV Op amps.

bit 0 **Unimplemented:** Read as 0

Reserved for future use.

**TABLE 4-3: CODE WORD LEVELS**

| DAC <7:5> | $V_{REF}$ | $V_{PP}$ (V) |
|---|---|---|
| 000 | 0.30 $V_{REF}$ | 67.5 |
| 001 | 0.40 $V_{REF}$ | 90 |
| 010 | 0.50 $V_{REF}$ | 112.5 |
| 011 | 0.60 $V_{REF}$ | 135 |
| 100 | 0.70 $V_{REF}$ | 157.5 |
| 101 | 0.80 $V_{REF}$ | 180 |
| 110 | 0.90 $V_{REF}$ | 202.5 |
| 111 | 1.00 $V_{REF}$ | 225 |

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#### 4.2.13.2 TRANSMIT REGISTER (TXB)

**TABLE 4-4: TRANSMIT REGISTER (TXB)**

| R-0 | R-0 | R-0 | R-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| — | | | | TEMP | SHORT | OVER | READY |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-4 **Unimplemented:** Read as 0

Reserved for future use.

bit 3 **TEMP:** Temperature Sensor Flag

1 = Junction temperature in the device has reached +125 °C to +150 °C.

0 = Junction temperature in the device is within the recommended operating range.

Note: The temperature sensor has a +25°C hysteresis. This is only an indicator flag and will not perform any actions to the DC-to-DC Controller or HV Amplifiers.

bit 2 **SHORT:** Short Circuit Flag

1 = Short Circuit detected, the DC-to-DC Controller suspends operation.
0 = Short Circuit NOT detected.

**Short Circuit Case:**

If SHT_EN = 1 and EN = 1 (in RXB Register); and if short circuit is detected, **SHORT =** 1. SHORT flag will be cleared on the **falling** edge (1 to 0) of EN (Bit 2 in RXB Register).

Note: If SHT_EN = 0 and EN = 0 or 1, in RXB Register, SHORT = 0.

bit 1 **OVER:** Overvoltage Flag

1 = $V_{PP}$ voltage is above 8% of its maximum recommended value, 225V. The DC-to-DC Controller suspends operation.

0 = $V_{PP}$ voltage is within the recommended operating range: 67.5V to 225V.

bit 0 **READY:** $V_{PP}$ Voltage

1 = $V_{PP}$ is OK for the HV Amplifier for operation.

0 = $V_{PP}$ is not ready for the HV Amplifier for operation.


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## DC/DC CONVERTER MODE OF OPERATION

| DC/DC Mode | Input | | | | Output | | | | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | EN | STD_BY | SHT_EN | SHDN | TEMP | SHORT | OVER | READY | |
| Enable | 1 | X | X | X | X | X | X | X | Enable DC/DC converter |
| Enable | 0 | X | X | X | X | 0 | 0 | 0 | Disable DC/DC converter |
| Standby | 1 | 1 | X | X | X | X | X | X | No PWM pulse to power FET. All the other DC/DC converter circuit is ON. |
| Shutdown | 1 | X | X | 1 | X | X | X | X | All amplifiers are turned off. Drivers are drawing minimum quiescent current for power saving. |
| Short Circuit | 1 | X | 1 | X | X | X | X | X | Short Circuit Protection ON |
| Overtemp. | X | X | X | X | 1/0 | X | X | X | 1: Overtemperature detected<br>0: No Overtemperature detected |
| Overvoltage | 1 | X | X | X | X | X | 1/0 | X | 1: Overvoltage detected<br>0: No Overvoltage detected |
| Short Circuit | 1 | X | 1 | X | X | 1/0 | X | X | 1: Short circuit detected<br>0: Short circuit NOT detected |
| Ready | 1 | X | X | X | X | X | X | 1/0 | 1: $V_{PP}$ OK to send data<br>0: $V_{PP}$ not OK to send data |

### 4.3 Power MOSFET

The internal Power MOSFET is a 60V device with a 10 mΩ Drain-to-Source ON resistance. The MOSFET is designed to be used in a flyback topology to generate up to 225V output voltage. The small input capacitance, Ciss, allows the topology to sustain a 480 kHz switching frequency.

The MOSFET is designed to generate up to 8 Watts of power during operation.


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## 5.0 APPLICATION INFORMATION

The HV56020 is designed for haptic applications where high voltage generation and integration are required. The device offers a complete solution by providing a DC-to-DC converter, a Power MOSFET, and HV Operational Amplifiers. The HV56020 is a battery operated device with an input voltage range of 2.7 to 5.5V.

In haptic applications, communication with the user occurs via the skin's haptic sensory system. Electro-Mechanical Polymer (EMP) Actuators are used in the low frequency band to stimulate the skin's sensory system. The haptic sensory system band frequency range is targeted around 1 Hz to 200 Hz and greater frequencies are used for audible feedback. The HV56020 is designed to drive 0.22 uF actuators at 124 Hz (-3 dB Bandwidth) with 225V sinusoidal waveforms.

Haptic applications require multiple channels to cover parts of the body with susceptible haptic sensory systems. For multiple channel solutions where simultaneous data transmission is not a strict requirement, the HV56022 can be used to add extra channel drive capacity. The HV56022 is a Dual High Voltage Operational Amplifier with the identical AC and DC electrical characteristics as the HV56020 amplifiers. The HV56020's $V_{DD}$ and $V_{LL}$ output voltages can be used to power HV56022's input voltage sources: $V_{CC}$ ($V_{DD}$) and $V_{LL}$.

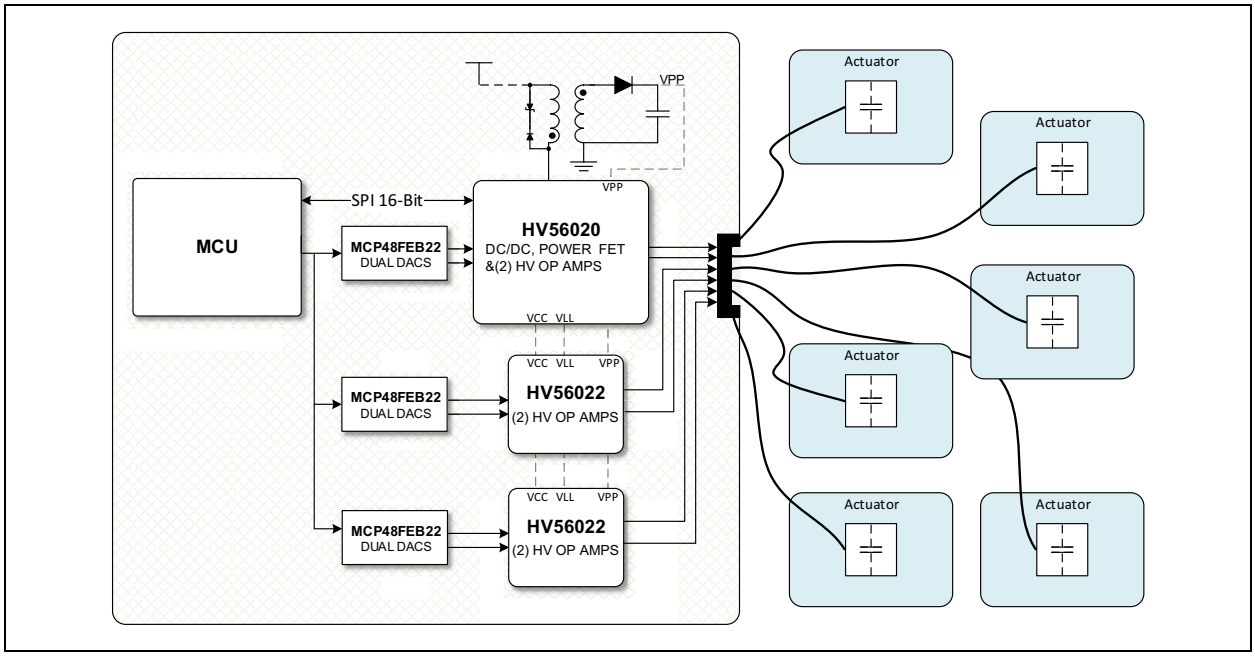


***FIGURE 5-1:*** *Application Block Diagram.*

## 5.1 PCB Layout Guidelines

The High Voltage Amplifiers can operate up to 225V with a 2.5 mA quiescent current ($I_{PPQ}$) during the idle state mode, dissipating 0.56 watts. During the transmission mode, the peak power can reach up to 3.7 watts ($I_{PP}$ 16.5 mA typical) when driving both HV Amplifiers simultaneously with a 0.22 µF load using a 124 Hz sine wave. Average and peak power levels depend on the load capacitance and the input data waveform characteristics: frequency, amplitude, rise/fall times and duration. The printed circuit board (PCB) layout design must accommodate for high power dissipation by having a low thermal resistance with the device, HV56020.

During normal operation, actuators are expected to operate in burst modes with intermittent idle times, allowing for moderate power consumptions. Power consumption becomes a concern for the continuous mode of operation, where each amplifier can dissipate up to 1.8 watts of instantaneous power. Continuous operation modes will lead to high power consumption and, in case of a poorly designed PCB, thermal runaway.

### 5.1.1 HV56020

The HV56020 is a multi-chip module consisting of three devices: (1) Dual High Voltage Operational Amplifiers, (2) a DC-to-DC Converter Controller, and (3) a Power MOSFET. The HV Amplifiers and the DC-to-DC controller sit on the package lead frame **Pad 1** connected to High Voltage Ground, **HVGND**. The Power MOSFET sits on **Pad 2** connected to the **Drain**. Most of the heat generated by the devices will flow via the package lead frame Pad 1 and Pad 2, and a minor heat portion via the package mold compound (and to the air via convection).

### 5.1.2 PCB LAYOUT

The thermal resistance from the device's silicon→ die attach → Pad1,2→PCB must be minimal to pull the heat out of the package as fast as possible. Low thermal resistance is achieved by the exposure of the pad's connections to a significant quantity of copper. It is recommended to use numerous **via** connections to the internal planes (HVGND and Drain connections) and to employ copper pour technique at the Top and Bottom Layers connecting the pads. Figure 5-2 illustrates the suggested layout for the copper pour and via connections in Top-Layer for Pad 1 and Pad 2**.**

The HVGND copper pour must be continuous throughout most of the PCB Top-Layer and regions containing the HV56020. HVGND connection pathways 1, 2, 3, and 4 must be cleared of components and signal traces to avoid cutting the ground plane and reducing the copper content in the Top Layer (see Figure 5-2). Small footprint components, e.g., 0402 EIA size code, and routing signal traces in the inner layers are recommended. Components for the **RT, TON, Timer Delay** and $\mathbf{R_{BIAS}}$ pins must be placed out of the HVGND pathways or at the Bottom-Layer. Trace routing for VIN0,1, and the SPI Interface signals: SCK, SDI, SDO, $\overline{SS}$, can be placed in the inner layers to avoid cutting the top ground plane.

**Note:** The standoff - spacing - for high voltage signal must be maintained in all layers/planes in accordance with the UL 840 pollution level 1, where a 0.56 mm minimum creepage spacing is recommended for 250V DC or AC RMS operation.

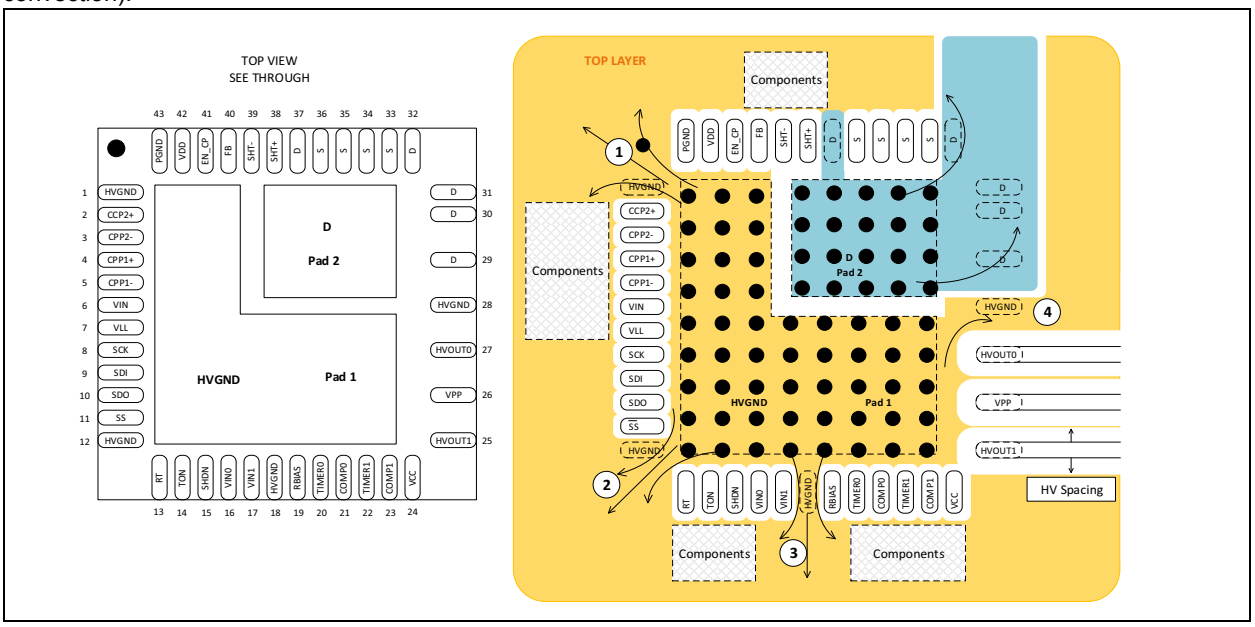


***FIGURE 5-2:*** *HV56020 PCB Layout Diagram.*


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### 5.1.3 PCB STACK-UP

The PCB is recommended to have a Stack-Up with at least four layers or higher count preferably to increase the ground (HVGND) copper content and help with the heat dissipation. The **Top** and **Bottom Layers** must be **2 Oz.** The rest of the planes and layers can be 1 Oz.

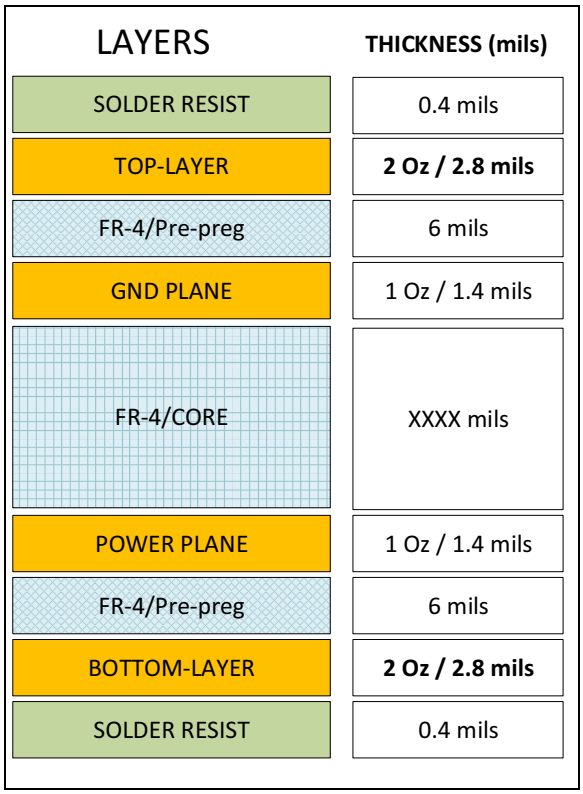
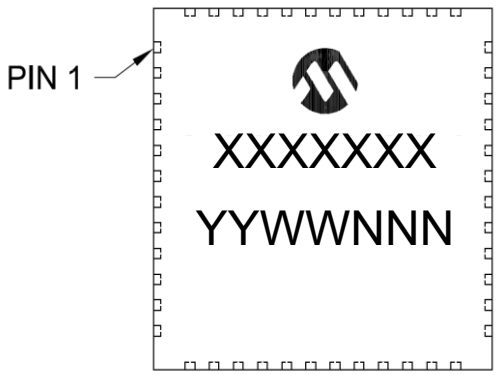



***FIGURE 5-3:*** *PCB Stack-Up.*

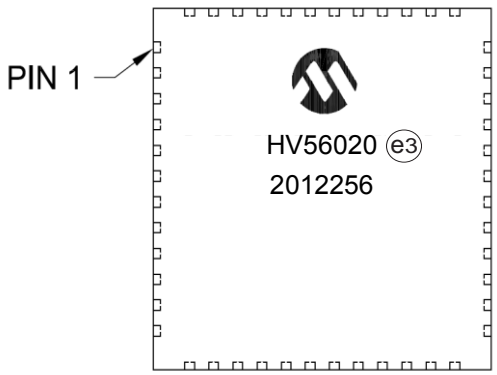
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

43-Lead VQFN




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.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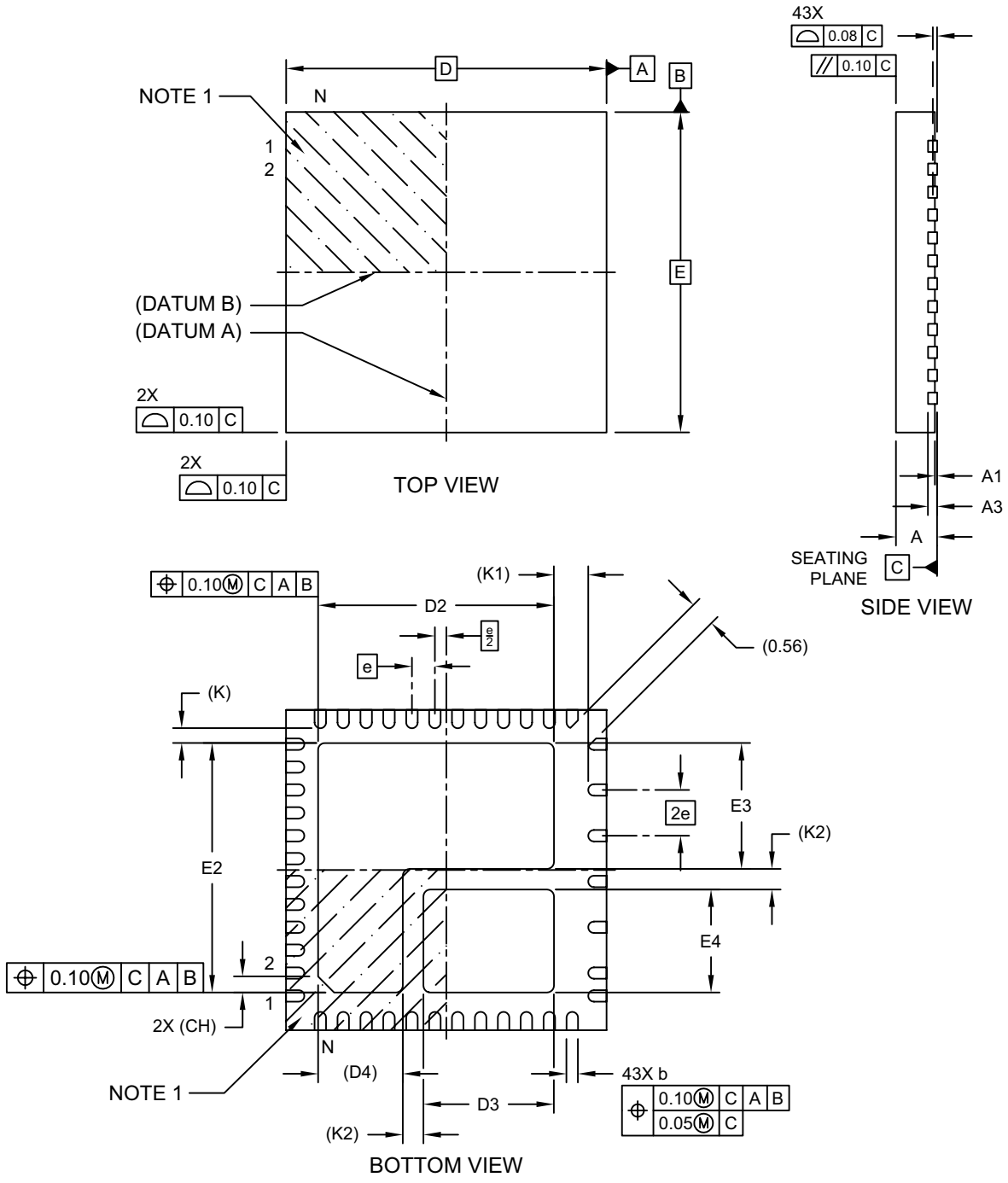
## 43-Lead Very Thin Plastic Quad Flat, No Lead Package (KXX) - 7x7 mm Body [VQFN] With Dual Exposed Pads

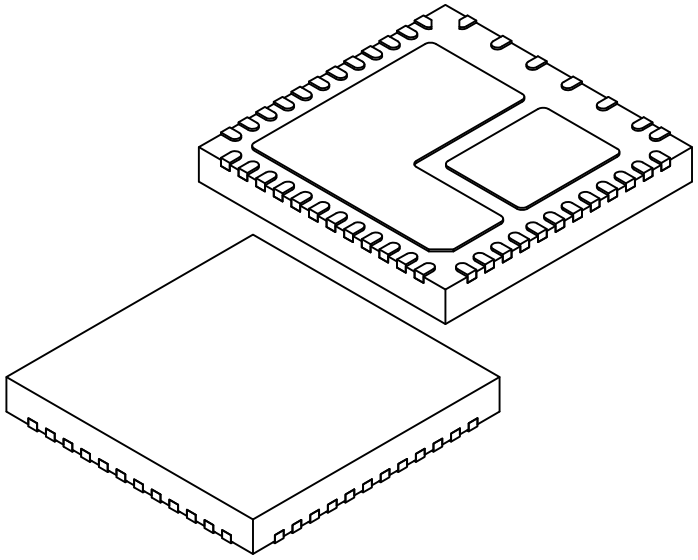
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-471 Rev. A Sheet 1 of 2

## 43-Lead Very Thin Plastic Quad Flat, No Lead Package (KXX) - 7x7 mm Body [VQFN] With Dual Exposed Pads

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 43 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 7.00 BSC | |
| Exposed Pad Length | D2 | 5.05 | 5.15 | 5.25 |
| Exposed Pad Length | D3 | 2.75 | 2.85 | 2.95 |
| Exposed Pad Length | D4 | | 1.85 REF | |
| Overall Width | E | | 7.00 BSC | |
| Exposed Pad Width | E2 | 5.35 | 5.45 | 5.55 |
| Exposed Pad Width | E3 | 2.65 | 2.75 | 2.85 |
| Exposed Pad Width | E4 | 2.15 | 2.25 | 2.35 |
| Terminal Width | b | 0.18 | 0.25 | 0.30 |
| Terminal Length | L | 0.35 | 0.40 | 0.45 |
| Pin 1 Index Chamfer | CH | | 0.35 REF | |
| Terminal-to-Exposed Pad | K | | 0.32 REF | |
| Terminal-to-Exposed Pad | K1 | | 0.75 REF | |
| Exposed Pad-to-Exposed Pad | K2 | | 0.45 REF | |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-471 Rev. A Sheet 2 of 2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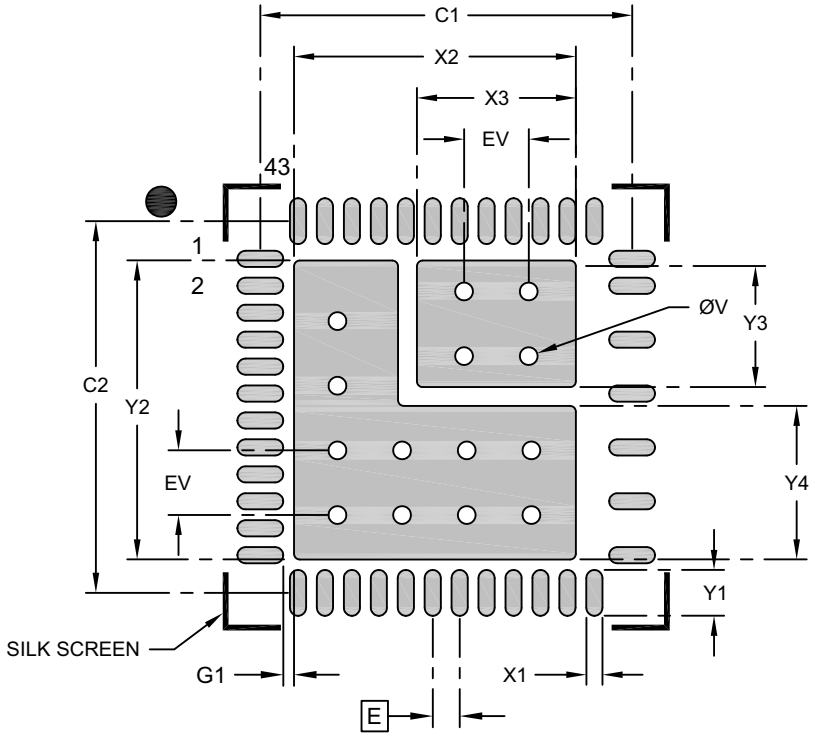
### 43-Lead Very Thin Plastic Quad Flat, No Lead Package (KXX) - 7x7 mm Body [VQFN] With Dual Exposed Pads

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 5.23 |
| Optional Center Pad Width | X3 | | | 2.95 |
| Optional Center Pad Length | Y2 | | | 5.55 |
| Optional Center Pad Length | Y3 | | | 2.35 |
| Optional Center Pad Length | Y4 | | | 2.85 |
| Contact Pad Spacing | C1 | | 6.90 | |
| Contact Pad Spacing | C2 | | 6.90 | |
| Contact Pad Width (X43) | X1 | | | 0.30 |
| Contact Pad Length (X43) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X43) | G1 | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2471 Rev. A

**NOTES:**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# APPENDIX A: REVISION HISTORY

## Revision A (March 2020)

- Initial release of this document

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X[1] | –X | /XXX |
|---|---|---|---|
| Device | Media Type | Temperature Range | Package |

| | | | |
|---|---|---|---|
| **Device:** | HV56020 | = | Dual High Voltage Op Amp with Step-Up Converter and Power MOSFET |
| **Media Type:** | T | = | 3000/Reel for KXX Package |
| **Temperature Range:** | V | = | 0°C to +125°C(Industrial)<br>Lead (Pb)-free/RoHS Compliant |
| **Package:** | KXX | = | Very Thin Quad Flatpack, No Lead 43-Terminal, 7 x 7 x 0.9 mm VQFN |

**Example:**

a) HV56020T-V/KXX = 43-Terminal VQFN, Industrial Temperature, Very Thin Quad Flatpack, No Lead, 3000/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**


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