DAC2932 12-Bit Dual Channel DAC EVM

This preliminary user's guide document gives a general overview of the DAC2932 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

Note:

This is a preliminary copy of the DAC2932 EVM User's Guide. This copy is to assist the user with the operation of the EVM using a SAMPLE DAC2932 device.

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1 Overview

1.1 Purpose

The DAC2932 EVM provides a platform for evaluating the DAC2932 digital-to-analog converter (DAC) under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Digital inputs for both current DAC's (I-DAC's) can be provided with CMOS level signals up to 80 MSPS through a 34 pin, 0.100 inch pitch header.

The serial interface for writing data to the four voltage DAC's (V-DAC's) is provided through three 2-pin headers.

The analog output from the I-DAC's are available via SMA connectors. Because of its flexible design the analog output of the DAC2932 can be configured to drive a 50-Ω terminated cable using a 16:1 impedance ratio transformer or single-ended referenced to GND.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog and digital supplies.

In addition to the internal bandgap reference provided by the DAC2932 device, an option is provided on the EVM to allow an external reference to be provided to the DAC.

1.3 Power Requirements

The demonstration board requires only a single power source. A power source of 3.3 V is required to be 3.3 VDC at banana jack J13 and J15 with the return going to either J14 or J16. J15 and J16 provides the analog supply for the DAC2932, while J13 and J14 provides the digital supply for the DAC2932. The EVM can be powered using only one supply, but powering from separate supplies will provide higher performance.

Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Under voltage may cause improper operation of some or all of the EVM components.

1.4 DAC2932 EVM Operational Procedure

The DAC2932 EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The demonstration board comes with following factory-set configuration:

- Single-ended clock source using a clock input at J1. Header J10 clock input is disabled (R27 is not installed).
- Transformer coupled outputs using transformer T1 and T2.
- I-DAC's set to operate with internal reference. REFIN decoupled to GND.
- V-DAC's set to operate with max reference. REFV jumper on W5 is installed between pins 2 and 3.
- Full-scale output current set to 2 mA through FSA1 resistor R3 (GSET jumper on W9 installed between pins 1 and 2).
- The I-DAC output's are enabled (power down mode disabled). PD jumper on W6 is installed between pins 1 and 2.
- The V-DAC output's are disabled (power down mode enabled). PDV jumper on W4 is installed between pins 2 and 3.
- I-DAC standby mode disabled. STBY_ jumper on W7 is installed between pins 2 and 3.
- I-DAC chip select mode enabled. CS_ jumper on W8 is installed between pins 1 and 2. Header J10 CS_ input is disabled (R28 is not installed).

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is attached at the end of this document.

2.2 Circuit Function

The following paragraphs describe the EVM circuits.

2.2.1 Input Clock

The DAC2932 EVM default operation setting is with a single-ended input clock sent to the DAC2932 from SMA connector J1. A 3 V p-p, 1.5-V offset, 50% duty cycle external square wave should be used. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC2932 converter, the clock source should feature low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance. An option is provided to operate the DAC with a clock source from header J10. When using J10 to provide the DAC clock, R27 must be installed and the clock amplitude must meet the requirements of the data sheet. If R1 is not removed, a voltage divider will be created with RP2.

2.2.2 Input Data

The DAC2932 EVM accepts 3.3-V CMOS logic level data inputs through the 34-pin header J10 per Table 1. RP1 and RP2 provide series dampening resistors to minimize digital ringing and switching noise. The default values are 22 Ω.

Table 1. Input Connector J10

J10 Pin No.	Description	J10 Pin No.	Description
1	Data Bit 11 (MSB)	18	GND
2	GND	19	Data Bit 2
3	Data Bit 10	20	GND
4	GND	21	Data Bit 1
5	Data Bit 9	22	GND
6	GND	23	Data Bit 0
7	Data Bit 8	24	GND
8	GND	25	
9	Data Bit 7	26	GND
10	GND	27	Chip Select
11	Data Bit 6	28	GND
12	GND	29	
13	Data Bit 5	30	GND
14	GND	31	
15	Data Bit 4	32	GND
16	GND	33	Clock
17	Data Bit 3	34	GND

2.2.3 Output Data

The DAC2932 EVM can be configured to drive a doubly terminated 50-Ω cable using a RF transformer or provide unbuffered differential outputs.

2.2.3.1 Transformer Coupled Signal Output

The factory-set configuration of the demonstration board provides the user with a single-ended output signal at SMA connectors J2 and J4. The DAC2932 is configured to drive a doubly terminated 50-Ω cable using a 16:1 impedance ratio transformer and the center tap of T1 and T2 connected to ground per Table 2. When not using a transformer, configure the EVM per Table 2.

Table 2. Transformer Output Configuration

CONFIGURATION	COMPONENTS INSTALLED(1)	COMPONENTS NOT INSTALLED
16:1 Impedance ratio transformer	R4–R7, R21, R23, T1, T2	R13–R20, R22, R24
Differential Outputs	R4–R7 (249), R14–R16, R18–R20	R13, R17, T1, T2

(1) All component values are per the schematic except where shown in parenthesis.

2.2.3.2 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows: Remove R13, R17, T1 and T2; Install R4–R7, R14–R16, and R18–R20.

2.2.4 I-DAC Internal Reference Operation

The full-scale output current is set by applying an external resistor ®$_{set}$) between the FSA pins of the DAC2932 and ground. The full-scale output current can be adjusted from 0.5 mA to 2 mA by varying R_{set} or changing the externally applied reference voltage. The full-scale output current, $IOUT_{FS}$, is defined as follows:

$$IOUT_{FS} = 32 \times (V_{ref} / R_{set})$$

where V_{ref} is the voltage at pin REF_{in}. This voltage is 1.22 V typical when using the internally provided bandgap reference voltage source. The full-scale output current on the DAC2932 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For independent settings, GSET must be tied high. On the DAC2932 EVM, with GSET high, R3 is used to set the output current of channel A and R2 is used to set channel B. With GSET tied low, both DAC output currents are controlled by R3.

2.2.5 I-DAC External Reference Operation

The I-DAC internal reference can be disabled by simply applying an external reference voltage into the REFin pin using Test Point 1. The use of an external reference may be considered for applications that require higher accuracy and drift performance. The reference input has a high impedance and can easily be driven by various sources.

The specified range for external reference voltages should be observed (see the DAC2932 data sheet for details).

2.2.6 V-DAC Internal Reference Operation

The reference voltage for the V-DAC's is set by the voltage applied to pin 43 (REFV). The output voltage provide by the V-DAC's is as follows:

$$V_{out} = REFV \times (D / 4096)$$

Where D = decimal equivalent of the binary code that is loaded into the DAC register. This value can range from 0 to 4095.

The specified range for REFV should be observed (see the DAC2932 data sheet for details).

2.2.7 Power Down Mode

The DAC2932 EVM provides a means of placing the I-DAC's and V-DAC's into a power-down mode. For the I-DAC's, this mode is activated by setting pin 16 (PD) high (jumper W6 between pins 2 and 3). For the V-DAC's, this mode is activated setting pin 44 (PDV) high (jumper W4 between pins 2 and 3).

2.2.8 Gain Set

The full-scale output current on the DAC2932 can be set two ways: both channels independently or simultaneously. For independent gain control, set GSET to a logic high (jumper W9 between pins 2 and 3). For simultaneous mode, set GSET to a logic low (W9 between pins 1 and 2).

2.2.9 Standby Mode

The DAC2932 EVM provides a means of placing the I-DAC's into a standby mode. This is activated by placing jumper W7 between pins 1 and 2.

2.2.10 Chip Select

The DAC2932 EVM provides a means of disabling the I-DAC's parallel data port with the use of a chipselect (CS_) signal. The parallel port is disabled when CS is set high (jumper W8 between pins 2-3)

3 Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

3.1 PCB Layout

The EVM is constructed on a 4-layer, 4.05-inch × 3.5-inch, 0.062-inch thick PCB using FR-4 material. Figure 1 through Figure 4 show the PCB layout for the EVM.

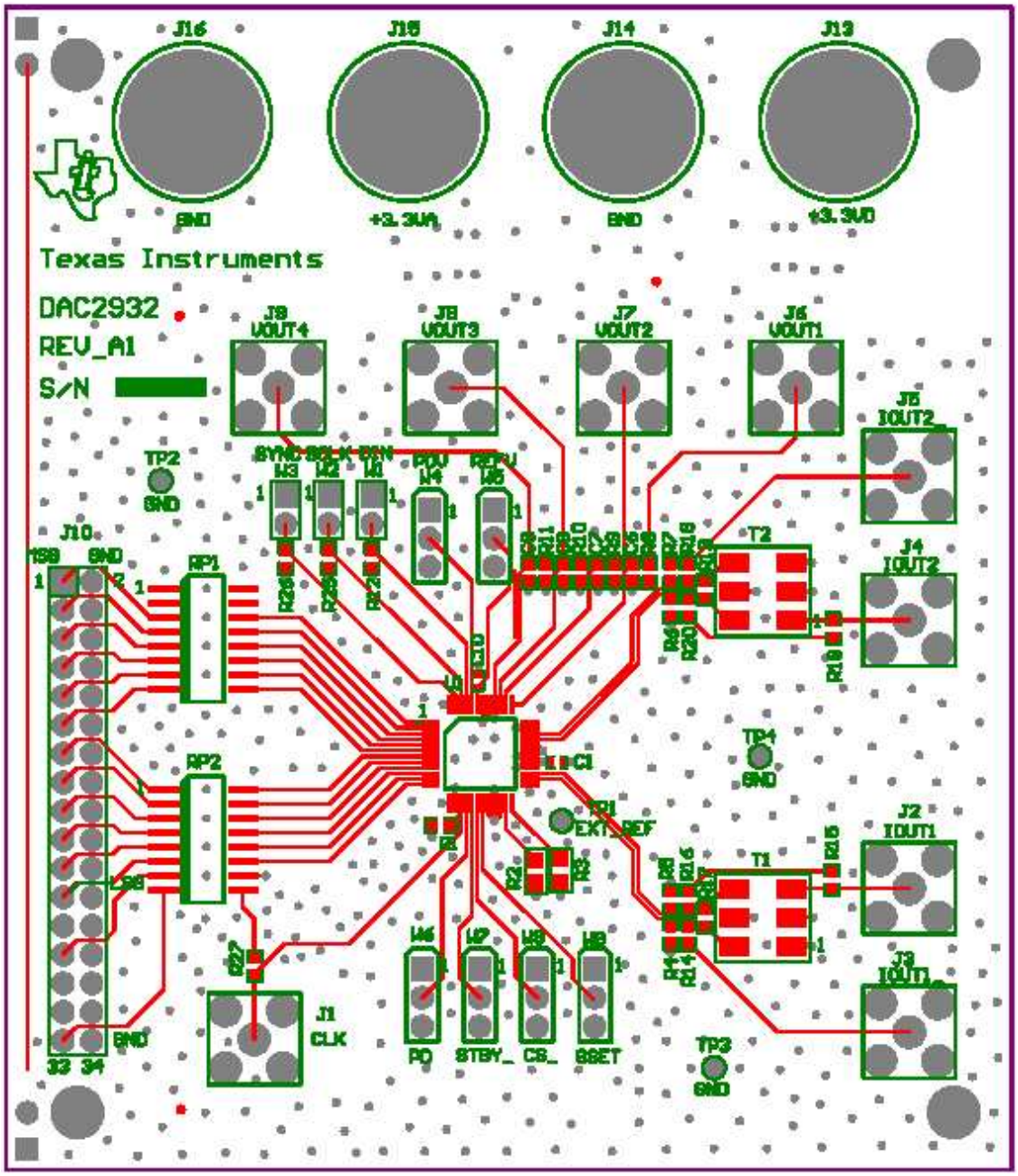

Figure 1. Top Layer 1

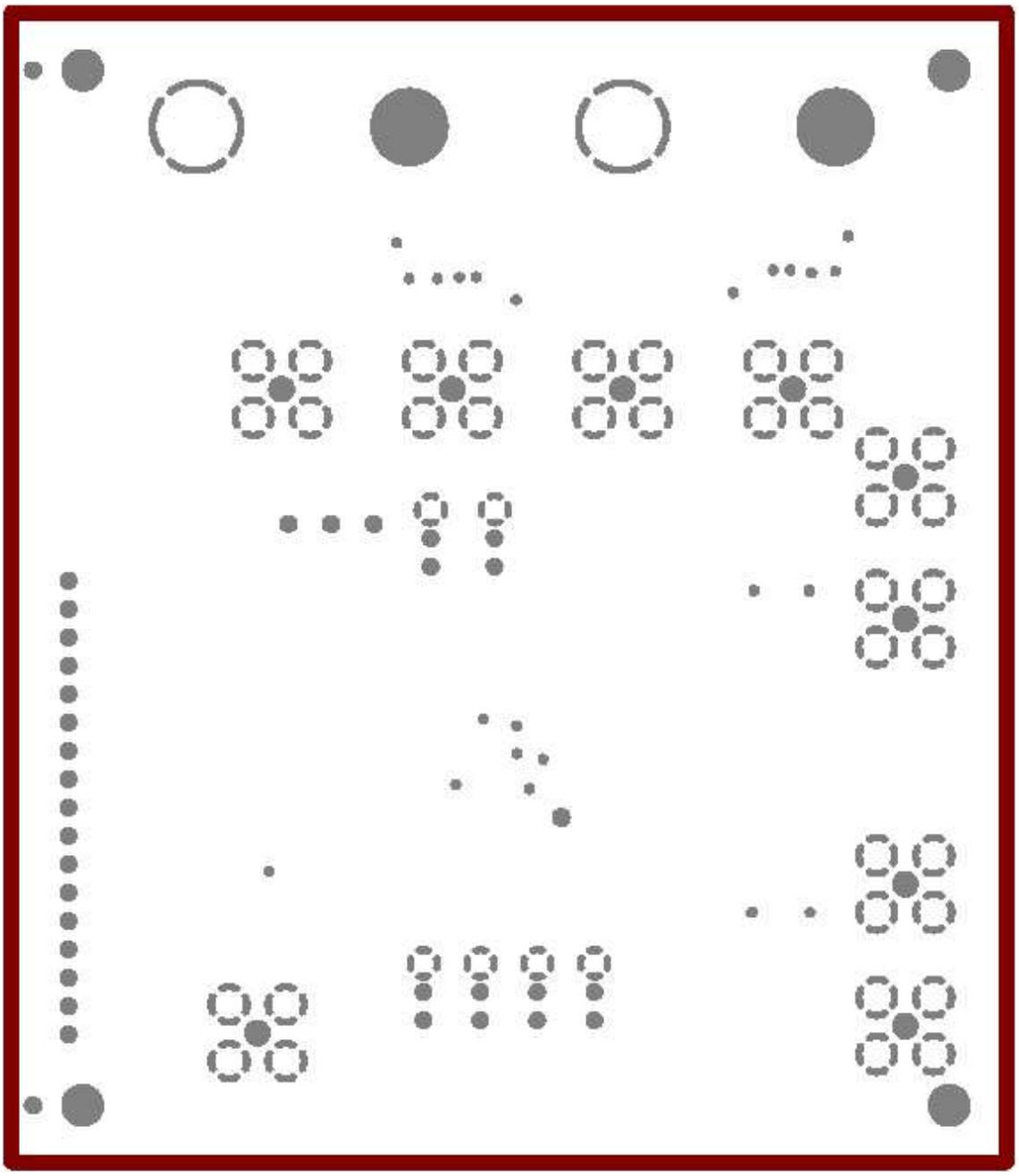

Figure 2. Layer 2, Ground Plane

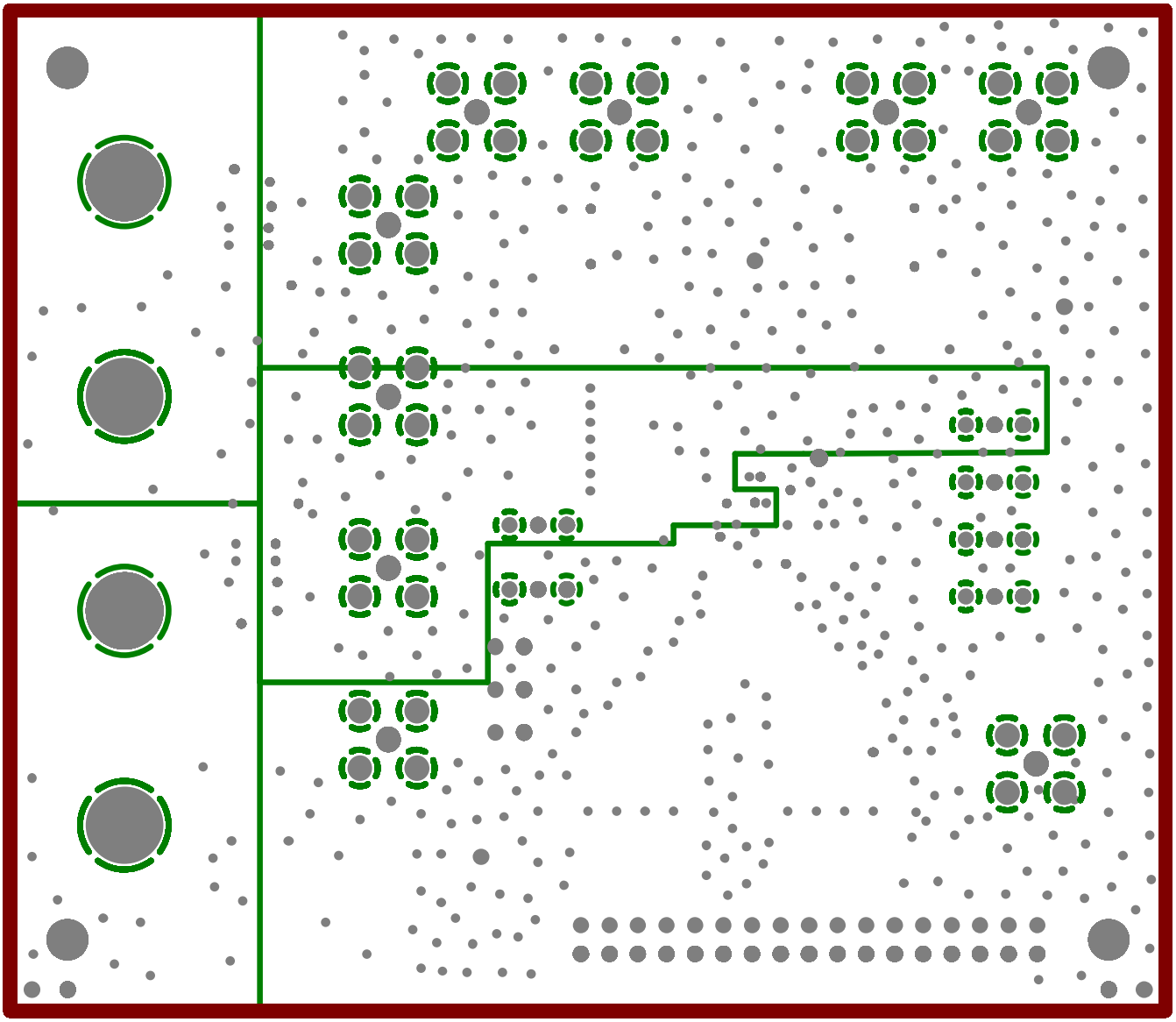

Figure 3. Layer 3, Power Plane

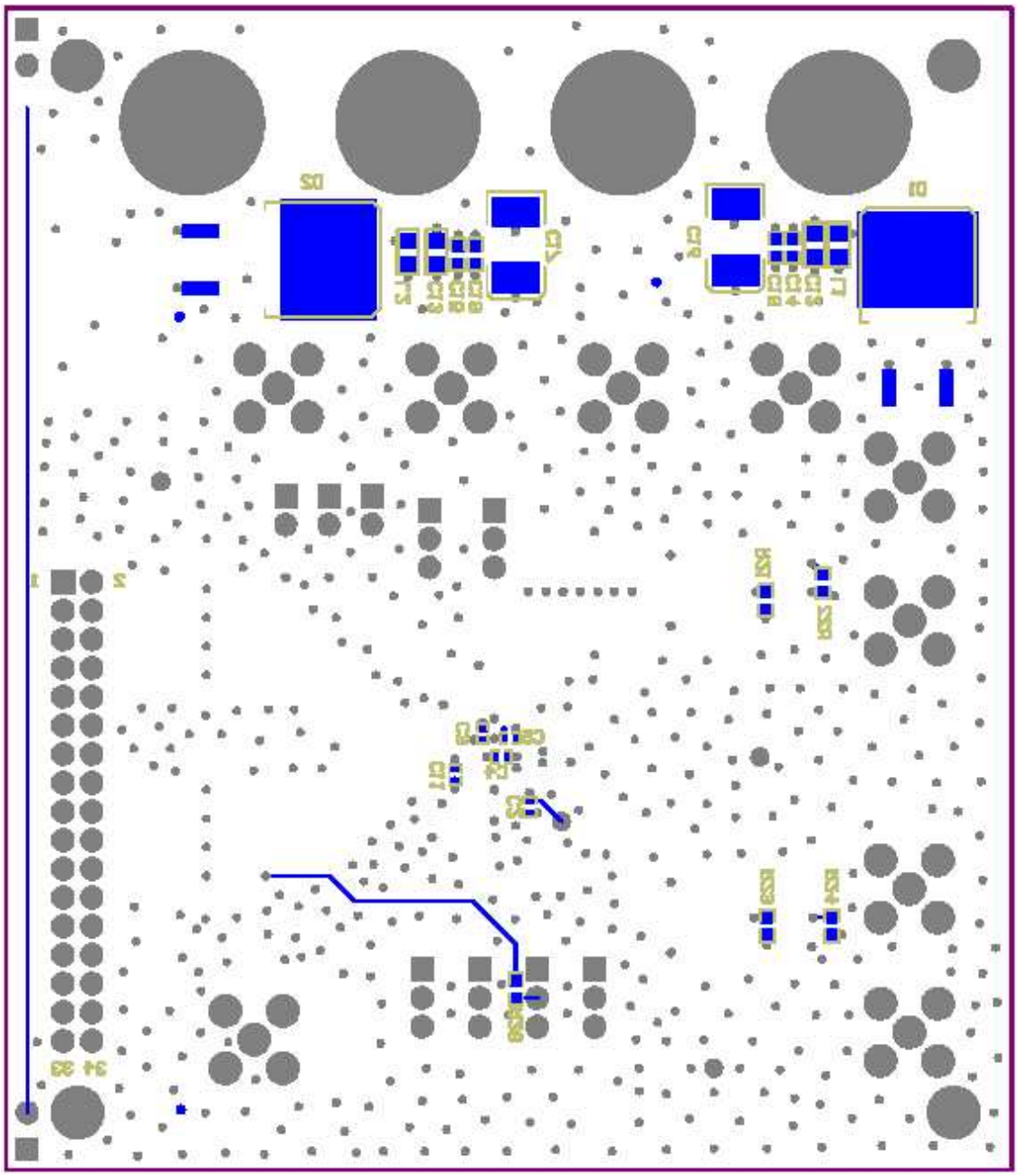

Figure 4. Layer 4, Bottom Layer

4 Parts List

Table 3 lists the parts used in constructing the EVM.

Table 3. DAC2932 EVM Parts List

Bill Of Material For DAC2932					
Value	**QTY**	**Part Number**	**Vendor**	**Ref Des**	**Not Installed**
CAPACITORS					
47 µF, 10 V, 20% Capacitor	2	ECS-T1AD476R	Murata	C16, C17	
0.1 µF, 25 V,10% Capacitor	2	ECJ-2VB1E104K	Panasonic	C12, C13	
0.001 µF, 50 V, 5% Capacitor	2	ECJ-1VC1H102J	Panasonic	C18, C19	
0.01 µF, 25 V, 10% Capacitor	2	ECJ-1VB1E103K	Panasonic	C14, C15	
0.1 µF, 25 V, 10% Capacitor	7	ECJ-1VB1E104K	Panasonic	C1, C2, C3, C4, C5, C10, C11	
39 pF, 50 µF, 5%Capacitor	4	ECJ-1VC1H390J	Panasonic	C6, C7, C8, C9	
RESISTORS					
19.6-kΩ resistor, 1/10 W, 1%	2	ERJ-6ENF1962V	Panasonic	R2, R3	
0-Ω resistor, 1/10 W, 5%	2	ERJ-3GEY0R00V	Panasonic	R21, R23	R14, R15, R16, R18, R19, R20, R22, R24, R27, R28
49.9-Ω resistor, 1/16 W, 1%	4	ERJ-3EKF49R9V	Panasonic	R1, R12, R25, R26	
402-Ω resistor, 1/16W, 0.1%	4	ERJ-3EKF4020V	Panasonic	R4, R5, R6, R7	R13, R17
2-kΩ resistor, 1/16 w, 1%	4	ERJ-3EKF2001V	Panasonic	R8, R9, R10, R11	
22-Ω resistor pack, 0.16 W, 1%	2	4816P-T01-220	Bourns	RP1, RP2	
FERRITE BEADS, CONNECTORS, JUMPER, JACKS, IC's, etc.					
Ferrite Bead	2	EXC-ML20A390U	Panasonic	L1, L2	
Red Test Point	1	5000K	Keystone	TP1	
Black Test Point	3	5001K	Keystone	TP2 TP3 TP4	
SMA connectors	9	901-144-8RFX	AMP	J1–J9	
2 POS_header	3	TSW-150-07-L-S	Samtec	W1 W2 W3	
3 POS_header	6	TSW-150-07-L-S	Samtec	W4–W9	
34-Pin header	1	TSW-117-07-L-D	Samtec	J10	
Red Banana Jacks	2	ST-351A	Allied	J13 J15	
Black Banana Jacks	2	ST-351B	Allied	J14 J16	
DAC2932PFB	1	DAC2932PFBT	Texas Instruments	U1	
Transformer	2	ADT16-6T	Mini-Circuits	T1 T2	
Diode	2	MBRB2515LT4	On Semiconductor	D1 D2	

4.1 Schematics

Figure 5 and Figure 6 contain the schematics for the DAC2932.

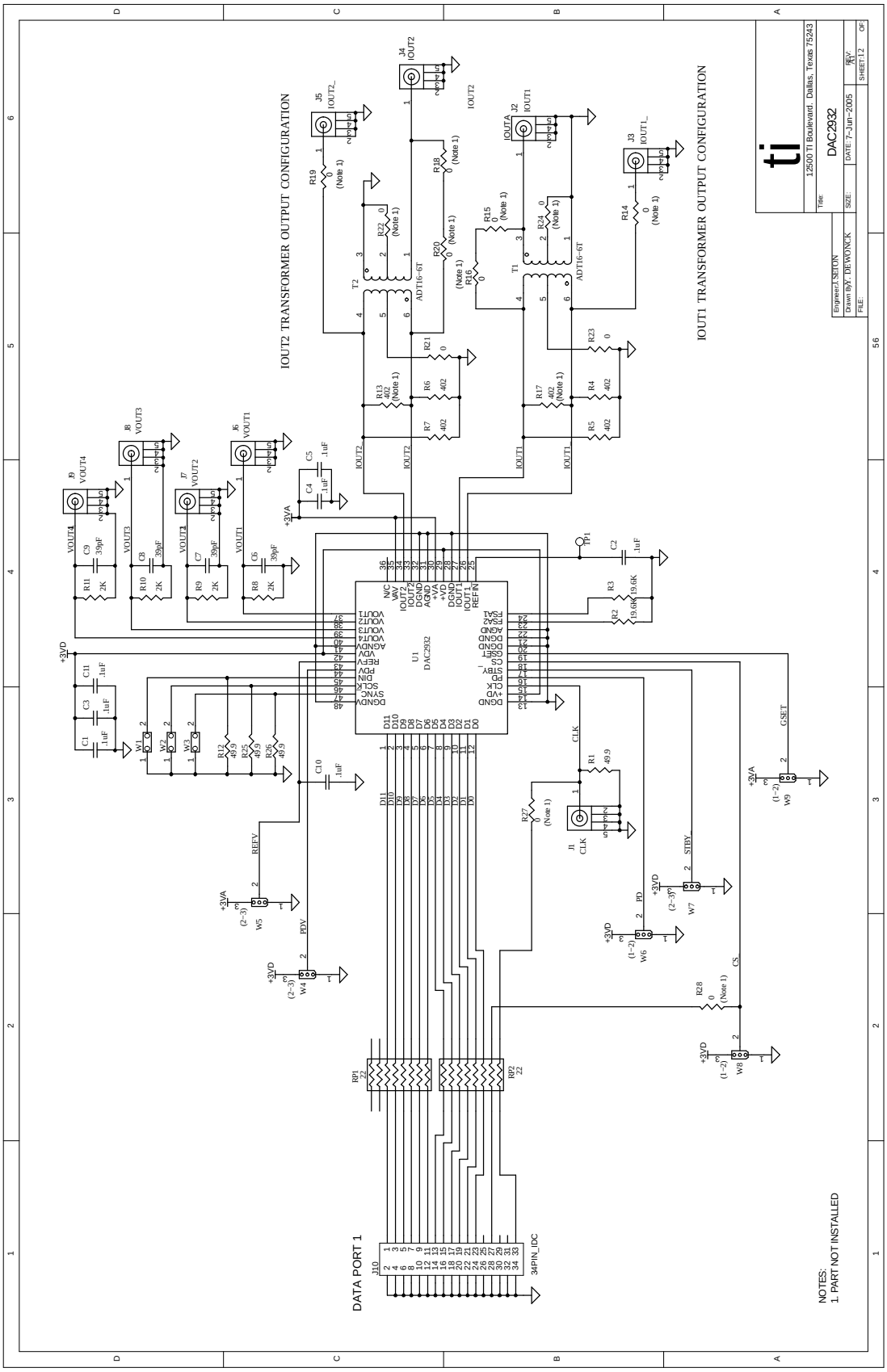

Figure 5. Schematic (Page 1)

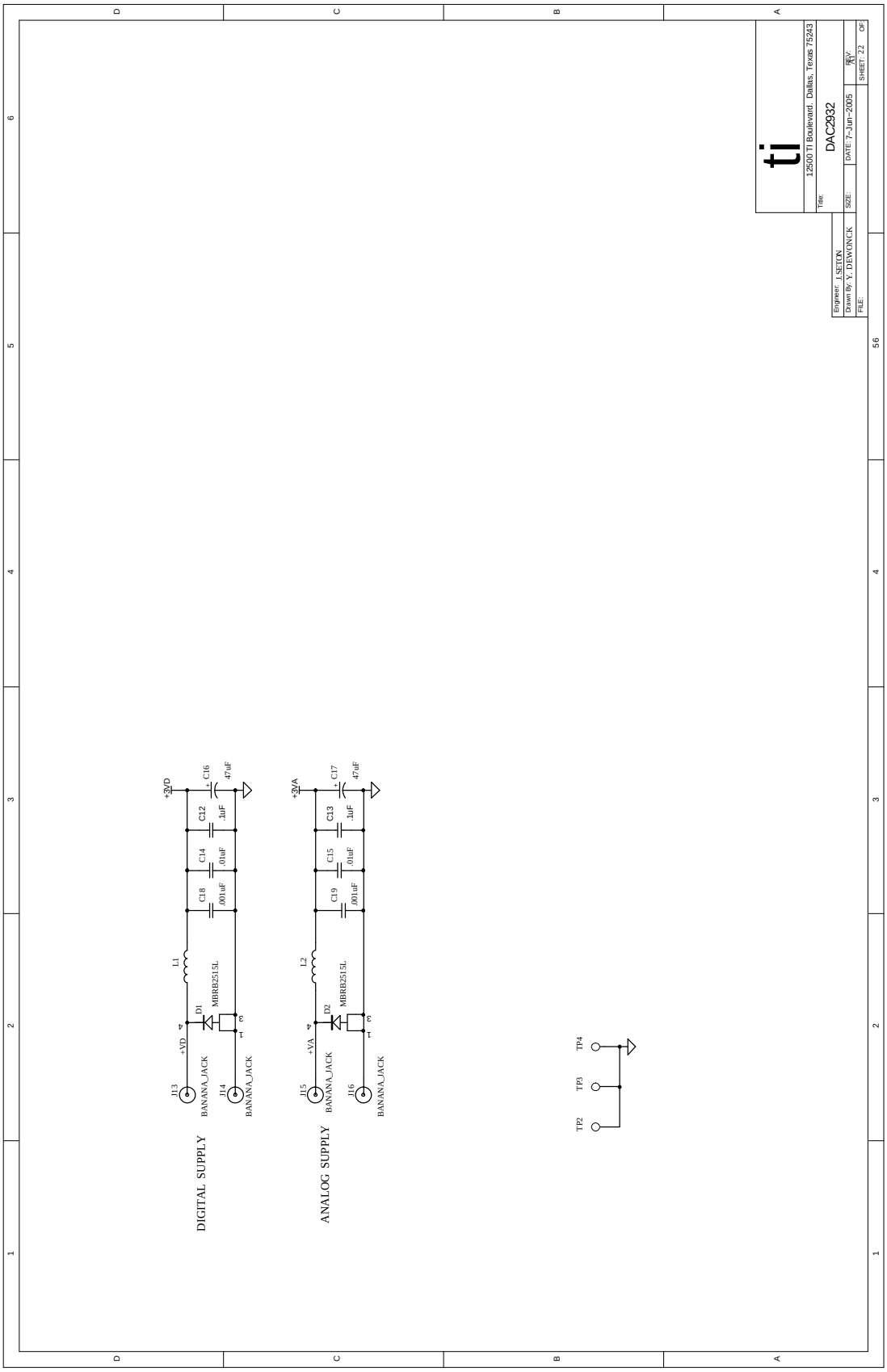

Figure 6. Schematic (Page 2)

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