

## Fast Infrared Transceiver Module (FIR, 4 Mbit/s) for 2.4 V to 3.6 V Operation and Low-Voltage Logic (1.8 V)

### Description

The TFDU6301 transceiver is an infrared transceiver module compliant to the latest IrDA physical layer low-power standard for fast infrared data communication, supporting IrDA speeds up to 4 Mbit/s (FIR), HP-SIR<sup>®</sup>, Sharp ASK<sup>®</sup> and carrier based remote control modes up to 2 MHz. Integrated within the transceiver module is a photo PIN diode, an infrared emitter (IRED), and a low-power control IC to provide a total front-end solution in a single package. This new Vishay FIR transceiver is built in a new smaller package using the experiences of the lead frame BabyFace technology. The transceivers are capable of directly interfacing with a wide variety of I/O devices, which perform the modulation/demodulation function. At a minimum, a  $V_{CC}$  bypass capacitor is the only external component required implementing a



complete solution. TFDU6301 has a tri-state output and is floating in shutdown mode with a weak pull-up. An otherwise identical transceiver with supply voltage related logic levels is available as TFDU6301.

### Features

- Compliant to the latest IrDA physical layer specification (up to 4 Mbit/s) with an extended low power range of > 70 cm (typ. 1 m) and TV remote control (> 9 m)
- Operates from 2.4 V to 3.6 V within specification
- Low power consumption (1.8 mA typ. supply current)
- Power shutdown mode (0.01  $\mu$ A typ. shutdown current)
- Surface mount package
  - Universal (L 8.5 mm x H 2.5 mm x W 3.1 mm)
- Tri-state-receiver output, floating in shut down with a weak pull-up



- Low profile (universal) package capable of surface mount soldering to side and top view orientation
- Directly interfaces with various super I/O and controller devices
- Only one external component required
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements saving costs
- Internal logic voltage reference of 1.8 V
- Lead (Pb)-free device
- Qualified for lead (Pb)-free and Sn/Pb processing (MSL4)
- Device in accordance with RoHS 2002/95/EC and WEEE 2002/96/EC

### Applications

- Notebook computers, desktop PCs, palmtop computers (Win CE, Palm PC), PDAs
- Digital cameras and video cameras
- Printers, fax machines, photocopiers, screen projectors
- Telecommunication products (cellular phones, pagers)
- Internet TV boxes, video conferencing systems
- External infrared adapters (dongles)
- Medical and industrial data collection

### Parts Table

Part	Description	Qty/reel or tube
TFDU6301-TR3	Oriented in carrier tape for side view surface mounting	2500 pcs
TFDU6301-TT3	Oriented in carrier tape for top view surface mounting	2500 pcs
TFDU6301-TR1	Oriented in carrier tape for side view surface mounting	750 pcs
TFDU6301-TT1	Oriented in carrier tape for top view surface mounting	750 pcs

## Product Summary

Parameter	Symbol	Value	Unit
Maximum data rate		4000	kbit/s
Dimensions	H x L x W	2.5 x 8.5 x 2.9	mm x mm x mm
Link distance		0 to $\geq 0.7$	m
Operating voltage	$V_{CC}$	2.4 to 3.6	V
Idle supply current	$I_{CC}$	2	mA

## Functional Block Diagram

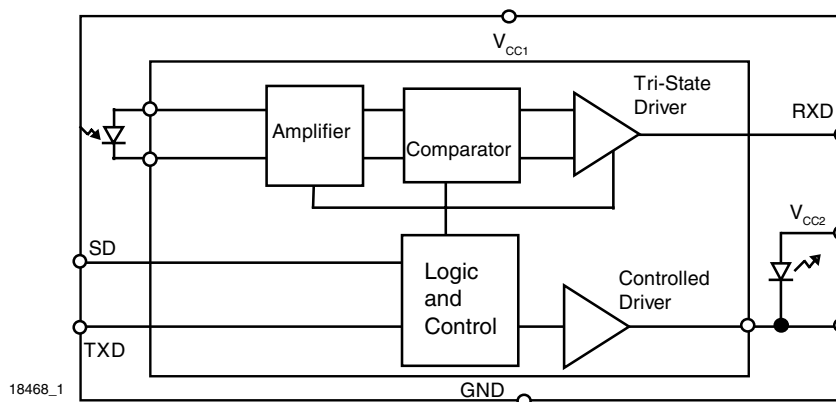


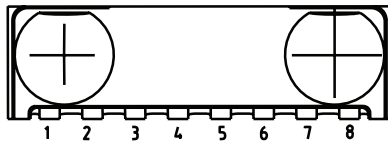
Figure 1. Functional Block Diagram

## Pin Description

Pin number	Function	Description	I/O	Active
1	$V_{CC2}$ IRED anode	IRED anode to be externally connected to $V_{CC2}$ ( $V_{IRED}$ ). For higher voltages than 3.6 V an external resistor might be necessary for reducing the internal power dissipation. This pin is allowed to be supplied from an uncontrolled power supply separated from the controlled $V_{CC1}$ - supply.		
2	IRED cathode	IRED cathode, internally connected to driver transistor		
3	TXD	This input is used to transmit serial data when SD is low. An on-chip protection circuit disables the IRED driver if the TXD pin is asserted for longer than 100 $\mu$ s. When used in conjunction with the SD pin, this pin is also used to control the receiver mode. Logic reference: 1.8 V logic	I	High
4	RXD	Received data output, push-pull CMOS driver output capable of driving standard CMOS. No external pull-up or pull-down resistor is required. Floating with a weak pull-up of 500 k $\Omega$ (typ.) in shutdown mode. High/low levels adapted to 1.8 V logic. RXD echoes the TXD signal.	O	Low
5	SD	Shutdown, also used for dynamic mode switching. Setting this pin active places the module into shutdown mode. On the falling edge of this signal, the state of the TXD pin is sampled and used to set receiver low bandwidth (TXD = low: SIR) or high bandwidth (TXD = high: MIR and FIR) mode.	I	High
6	$V_{CC1}$	Supply voltage		
7	NC	Internally not connected	I	
8	GND	Ground		

**Pinout**

Weight 0.075 g



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Figure 2. Pinning

**Definitions:**

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR low power standard. IrPhy 1.3 extended the low power option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version. With introducing the updated versions the old versions are obsolete. Therefore the only valid IrDA standard is the actual version IrPhy 1.4 (in Oct. 2002).

**Absolute Maximum Ratings**

Reference point pin: GND unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range, transceiver	$0\text{ V} < V_{CC2} < 6\text{ V}$	$V_{CC1}$	- 0.5		6	V
Supply voltage range, transmitter	$0\text{ V} < V_{CC1} < 6\text{ V}$	$V_{CC2}$	- 0.5		6.5	V
Voltage at all I/O pins	$V_{in} < V_{CC1}$ is allowed		- 0.5		6	V
Input currents	For all pins, except IRED anode pin				10	mA
Output sinking current					25	mA
Power dissipation		$P_D$			500	mW
Junction temperature		$T_J$			125	°C
Ambient temperature range (operating)		$T_{amb}$	- 25		+ 85	°C
Storage temperature range		$T_{stg}$	- 25		+ 85	°C
Soldering temperature	See chapter "Recommended Solder Profiles"				260	°C
Average output current		$I_{IRED} (DC)$			150	mA
Repetitive pulse output current	$< 90\ \mu\text{s}$ , $t_{on} < 20\%$	$I_{IRED} (RP)$			700	mA
ESD protection	Human body model		1			kV

**Eye Safety Information**

Vishay transceivers operating inside the absolute maximum ratings are classified as eye safe according to the following table.

Standard	Classification
IEC/EN 60825-1 (2007-03), DIN EN 60825-1 (2008-05) "SAFETY OF LASER PRODUCTS - Part 1: equipment classification and requirements", simplified method	Class 1
IEC 62471 (2006), CIE S009 (2002) "Photobiological Safety of Lamps and Lamp Systems"	Exempt
DIRECTIVE 2006/25/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 5 <sup>th</sup> April 2006 on the minimum health and safety requirements regarding the exposure of workers to risks arising from physical agents (artificial optical radiation) (19 <sup>th</sup> individual Directive within the meaning of Article 16(1) of Directive 89/391/EEC)	Exempt

## Electrical Characteristics

## Transceiver

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC1} = V_{CC2} = 2.4\text{ V}$  to  $3.6\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		$V_{CC}$	2.4		3.6	V
Dynamic supply current	Receive mode only, idle In transmit mode, add additional 85 mA (typ) for IRED current. Add RXD output current depending on RXD load.					
	SIR mode	$I_{CC}$		1.8	3.0	mA
	MIR/FIR mode	$I_{CC}$		2.0	3.3	mA
Shutdown supply current	SD = high $T = 25\text{ }^{\circ}\text{C}$ , not ambient light sensitive, detector is disabled in shutdown mode	$I_{SD}$		0.01		$\mu\text{A}$
Shutdown supply current	SD = high, full specified temperature range, not ambient light sensitive	$I_{SD}$			1	$\mu\text{A}$
Operating temperature range		$T_A$	- 25		+ 85	$^{\circ}\text{C}$
Digital Reference Voltage	Internally generated	$V_{dd}$	1.62	1.8	1.98	V
Input voltage low (TXD, SD)		$V_{IL}$	- 0.5		0.5	V
Input voltage high <sup>(1)</sup> (TXD, SD)		$V_{IH}$	1.5	1.8	6	V
Input leakage current (TXD, SD)	$V_{in} > 1.6\text{ V}$	$I_{ICH}$	- 1		+ 1	$\mu\text{A}$
Input capacitance, TXD, SD		$C_I$			5	pF
Output voltage low	$I_{OL} = 500\text{ }\mu\text{A}$ $C_{load} = 15\text{ pF}$	$V_{OL}$			0.4	V
Output voltage high	$I_{OH} = - 250\text{ }\mu\text{A}$ $C_{load} = 15\text{ pF}$	$V_{OH}$	$0.8 \times V_{dd}$			V
Output RXD current limitation high state low state	Short to ground Short to $V_{CC1}$				20 20	mA mA
SD shutdown pulse duration	Activating shutdown		30		$\infty$	$\mu\text{s}$
RXD to $V_{CC1}$ impedance		$R_{RXD}$	400	500	600	k $\Omega$
SD mode programming pulse duration	All modes	$t_{SDPW}$	200			ns

Note:

<sup>(1)</sup> The typical threshold level is  $0.5 \times V_{dd}$ . It is recommended to use the specified min./max. values to avoid increased operating current.



## Optoelectronic Characteristics

### Receiver

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC1} = V_{CC2} = 2.4\text{ V}$  to  $3.6\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Minimum irradiance $E_e$ <sup>(1)</sup> in angular range <sup>(2)</sup>	9.6 kbit/s to 115.2 kbit/s $\lambda = 850\text{ nm}$ to $900\text{ nm}$ , $V_{CC} = 2.4\text{ V}$	$E_e$		50 (5)	80 (8)	$\text{mW}/\text{m}^2$ ( $\mu\text{W}/\text{cm}^2$ )
Minimum irradiance $E_e$ in angular range, MIR mode	1.152 Mbit/s $\lambda = 850\text{ nm}$ to $900\text{ nm}$ , $V_{CC} = 2.4\text{ V}$	$E_e$		100 (10)		$\text{mW}/\text{m}^2$ ( $\mu\text{W}/\text{cm}^2$ )
Minimum irradiance $E_e$ in angular range, FIR mode	4 Mbit/s $\lambda = 850\text{ nm}$ to $900\text{ nm}$ , $V_{CC} = 2.4\text{ V}$	$E_e$		130 (13)	200 (20)	$\text{mW}/\text{m}^2$ ( $\mu\text{W}/\text{cm}^2$ )
Maximum irradiance $E_e$ in angular range <sup>(3)</sup>	$\lambda = 850\text{ nm}$ to $900\text{ nm}$	$E_e$	5 (500)			$\text{kW}/\text{m}^2$ ( $\text{mW}/\text{cm}^2$ )
Rise time of output signal	10 % to 90 %, $C_L = 15\text{ pF}$	$t_r$ (RXD)	10		40	ns
Fall time of output signal	90 % to 10 %, $C_L = 15\text{ pF}$	$t_f$ (RXD)	10		40	ns
RXD pulse width of output signal, 50 %, SIR mode	Input pulse length $1.4\text{ }\mu\text{s} < P_{Wopt} < 25\text{ }\mu\text{s}$	$t_{PW}$	1.6	2.2	3	$\mu\text{s}$
RXD pulse width of output signal, 50 %, MIR mode	Input pulse length $P_{Wopt} = 217\text{ ns}$ , 1.152 Mbit/s	$t_{PW}$	105	250	275	ns
RXD pulse width of output signal, 50 %, FIR mode	Input pulse length $P_{Wopt} = 125\text{ ns}$ , 4 Mbit/s	$t_{PW}$	105	125	145	ns
RXD pulse width of output signal, 50 %, FIR mode	Input pulse length $P_{Wopt} = 250\text{ ns}$ , 4 Mbit/s	$t_{PW}$	225	250	275	ns
Stochastic jitter, leading edge	Input irradiance = $100\text{ mW}/\text{m}^2$ , 4.0 Mbit/s 1.152 Mbit/s $\leq 115.2\text{ kbit/s}$				25 80 350	ns ns ns
Receiver start up time	After completion of shutdown programming sequence power on delay				250	$\mu\text{s}$
Latency		$t_L$		40	100	$\mu\text{s}$

#### Note:

All timing data measured with 4 Mbit/s are measured using the IrDA<sup>®</sup> FIR transmission header. The data given here are valid 5  $\mu\text{s}$  after starting the preamble.

(1) IrDA low power specification is  $90\text{ mW}/\text{m}^2$ . Specification takes into account a window loss of 10 %.

(2) **IrDA sensitivity definition (equivalent to threshold irradiance): minimum irradiance  $E_e$  in angular range**, power per unit area. The receiver must meet the BER specification while the source is operating at the minimum intensity in angular range into the minimum half-angle range at the maximum link length.

(3) **Maximum irradiance  $E_e$  in angular range**, power per unit area. The optical power delivered to the detector by a source operating at the maximum intensity in angular range at minimum link length must not cause receiver overdrive distortion and possible related link errors. If placed at the active output interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER) specification.

For more definitions see the document "Symbols and Terminology" on the Vishay website.

## Transmitter

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC1} = V_{CC2} = 2.4\text{ V}$  to  $3.6\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

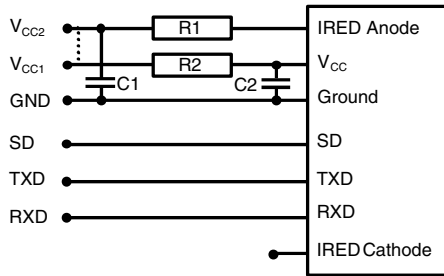
Parameter	Test conditions	Symbol	Min.	Typ.	Max.	Unit
IRED operating current, switched current limiter	Note: No external resistor current limiting resistor is needed	$I_D$	330	440	600	mA
Output pulse width limitation	Input pulse width $t < 20\text{ }\mu\text{s}$	$t_{pw}$		t		$\mu\text{s}$
	Input pulse width $20\text{ }\mu\text{s} < t < 150\text{ }\mu\text{s}$	$t_{pw}$	18		150	$\mu\text{s}$
	Input pulse width $t \geq 150\text{ }\mu\text{s}$	$t_{pw\_lim}$			150	$\mu\text{s}$
Output leakage IRED current		$I_{IRED}$	- 1		1	$\mu\text{A}$
Output radiant intensity, see figure 3, recommended appl. circuit	$V_{CC} = V_{IRED} = 3.3\text{ V}$ , $\alpha = 0^{\circ}$ TXD = high, SD = Low	$I_e$	65	180	468 <sup>(1)</sup>	mW/sr
Output radiant intensity, see figure 3, recommended appl. circuit	$V_{CC} = V_{IRED} = 3.3\text{ V}$ , $\alpha = 0^{\circ}$ , $15^{\circ}$ TXD = high, SD = Low	$I_e$	50	125	468 <sup>(1)</sup>	mW/sr
Output radiant intensity	$V_{CC1} = 3.3\text{ V}$ , $\alpha = 0^{\circ}$ , $15^{\circ}$ TXD = low or SD = high (Receiver is inactive as long as SD = high)	$I_e$			0.04	mW/sr
Output radiant intensity, angle of half intensity		$\alpha$		$\pm 24$		$^{\circ}$
Peak - emission wavelength <sup>(2)</sup>		$\lambda_p$	875	886	900	nm
Spectral bandwidth		$\Delta\lambda$		45		nm
Optical rise time, Optical fall time		$t_{ropt}$ , $t_{fopt}$	10		40	ns
Optical output pulse duration	Input pulse width 217 ns, 1.152 Mbit/s	$t_{opt}$	207	217	227	ns
Optical output pulse duration	Input pulse width 125 ns, 4 Mbit/s	$t_{opt}$	117	125	133	ns
Optical output pulse duration	Input pulse width 250 ns, 4 Mbit/s	$t_{opt}$	242	250	258	ns
Optical overshoot					25	%

Note:

- (1) Maximum value is given by eye safety class 1, IEC 60825-1, simplified method.
- (2) Due to this wavelength restriction compared to the IrDA spec of 850 nm to 900 nm the transmitter is able to operate as source for the standard Remote Control applications with codes as e.g. Philips RC5/RC6<sup>®</sup> or RECS 80. When operated under IrDA full range conditions (125 mW/sr) the RC range to be covered is in the range from 8 m to 12 m, provided that state of the art remote control receivers are used.

### Recommended Circuit Diagram

Operated at a clean low impedance power supply the TFDU6301 needs no additional external components. However, depending on the entire system design and board layout, additional components may be required (see figure 3).



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Figure 3. Recommended Application Circuit

The capacitor C1 is buffering the supply voltage and eliminates the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is only necessary for high operating voltages and elevated temperatures.

Vishay transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (TXD, SD) and the output RXD should be directly (DC) coupled to the I/O circuit.

The capacitor C2 combined with the resistor R2 is the low pass filter for smoothing the supply voltage.

R2, C1 and C2 are optional and dependent on the quality of the supply voltages  $V_{CCx}$  and injected noise. An unstable power supply with dropping voltage during transmission may reduce the sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as close as possible to the transceiver power supply pins. A Tantalum capacitor should be used for C1 while a ceramic capacitor is used for C2.

In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at  $V_{CC2}$ . Often some power supplies are not able to follow the fast current rise time. In that case another 4.7  $\mu$ F (type, see table under C1) at  $V_{CC2}$  will be helpful.

Keep in mind that basic RF-design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Winfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

**Table 1.**  
**Recommended Application Circuit Components**

Component	Recommended value	Vishay part number
C1	4.7 $\mu$ F, 16 V	293D 475X9 016B
C2	0.1 $\mu$ F, ceramic	VJ 1206 Y 104 J XXMT
R1	No resistor necessary, the internal controller is able to control the current	
R2	10 $\Omega$ , 0.125 W	CRCW-1206-10R0-F-RT1

**I/O and Software**

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

**Mode Switching**

The TFDU6301 is in the SIR mode after power on as a default mode, therefore the FIR data transfer rate has to be set by a programming sequence using the TXD and SD inputs as described below. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity. To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

**Setting to the High Bandwidth Mode (0.576 Mbit/s to 4 Mbit/s)**

1. Set SD input to logic "High".
2. Set TXD input to logic "High". Wait  $t_s \geq 200$  ns.
3. Set SD to logic "Low" (this negative edge latches state of TXD, which determines speed setting).
4. After waiting  $t_h \geq 200$  ns TXD can be set to logic "Low". The hold time of TXD is limited by the maximum allowed pulse length.

TXD is now enabled as normal TXD input for the high bandwidth mode.

**Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)**

1. Set SD input to logic "High".
2. Set TXD input to logic "Low". Wait  $t_s \geq 200$  ns.
3. Set SD to logic "Low" (this negative edge latches state of TXD, which determines speed setting).
4. TXD must be held for  $t_h \geq 200$  ns. TXD is now enabled as normal TXD input for the lower bandwidth mode.

Note:

When applying this sequence to the device already in the lower bandwidth mode, the SD pulse is interpreted as shutdown. In this case the RXD output of the transceiver may react with a single pulse (going active low) for a duration less than 2  $\mu$ s. The operating software should take care for this condition. In case the applied SD pulse is longer than 4  $\mu$ s, no RXD pulse is to be expected but the receiver startup time is to be taken into account before the device is in receive condition.

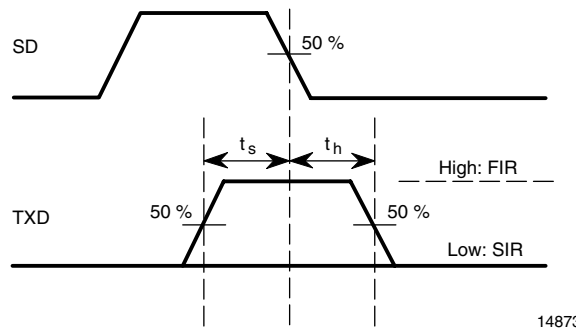


Figure 4. Mode Switching Timing Diagram

**Table 2. Truth table**

Inputs			Outputs	
SD	TXD	Optical input irradiance mW/m <sup>2</sup>	RXD	Transmitter
High	x	x	weakly pulled (500 k $\Omega$ ) to V <sub>CC1</sub>	0
Low	High	x	Low (echo)	I <sub>e</sub>
	High > 150 $\mu$ s	x	High	0
	Low	< 4	High	0
	Low	> Min. detection threshold irradiance < Max. detection threshold irradiance	Low (active)	0
	Low	> Max. detection threshold irradiance	x	0



## Recommended Solder Profiles

### Solder Profile for Sn/Pb Soldering

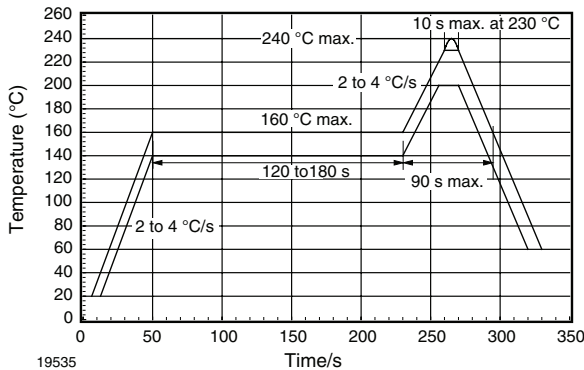


Figure 5. Recommended Solder Profile for Sn/Pb Soldering

### Lead (Pb)-free, Recommended Solder Profile

The TFDU6301 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn<sub>(3.0 - 4.0)</sub>Ag<sub>(0.5 - 0.9)</sub>Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 6 and 7 are VISHAY's recommended profiles for use with the TFDU6301 transceivers. For more details please refer to the application note "SMD Assembly Instructions" (<http://www.vishay.com/doc?82602>).

A ramp-up rate less than 0.9 °C/s is not recommended. Ramp-up rates faster than 1.3 °C/s could damage an optical part because the thermal conductivity is less than compared to a standard IC.

### Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

### Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

### Storage

The storage and drying processes for all VISHAY transceivers (TFDUxxxx and TFBSxxx) are equivalent to MSL4.

The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing".

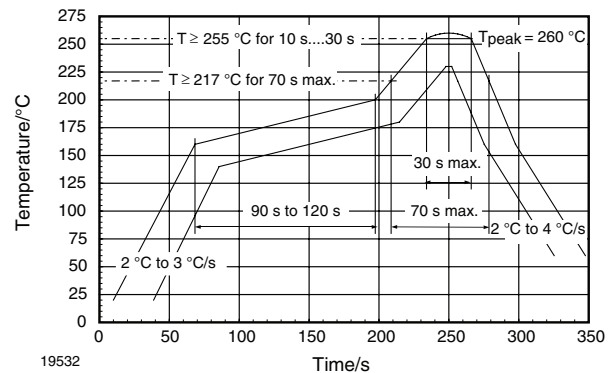


Figure 6. Solder Profile, RSS Recommendation

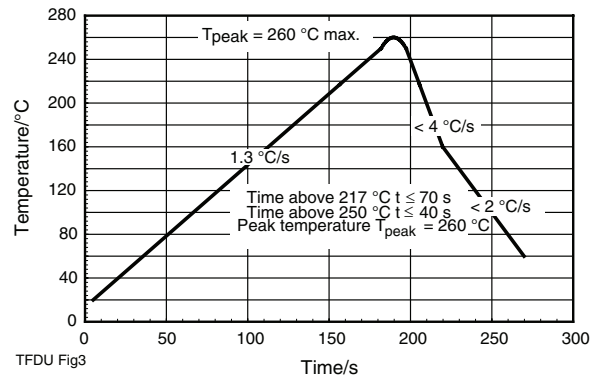
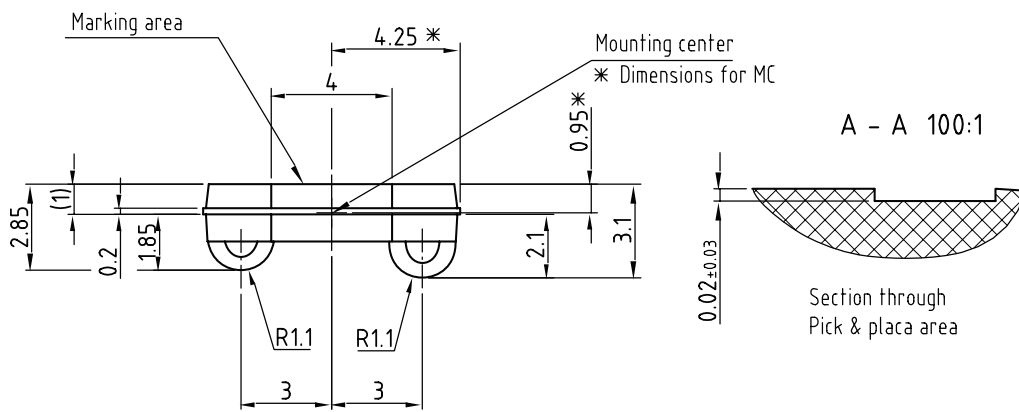
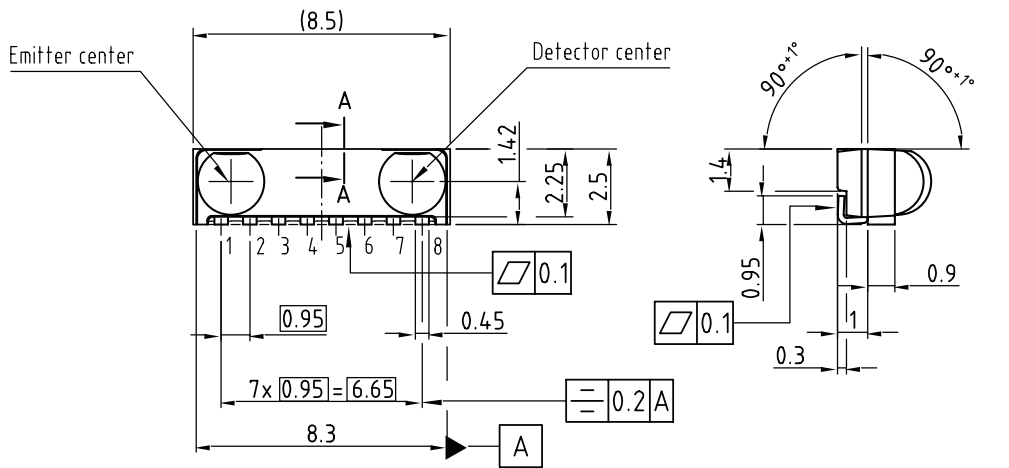


Figure 7. RTS Recommendation

Package Dimensions in mm  
TFDU6301 (Universal) Package



Drawing-No.: 6.550-5252.01-4  
Issue: 2; 12.10.04

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technical drawings  
according to DIN  
specifications

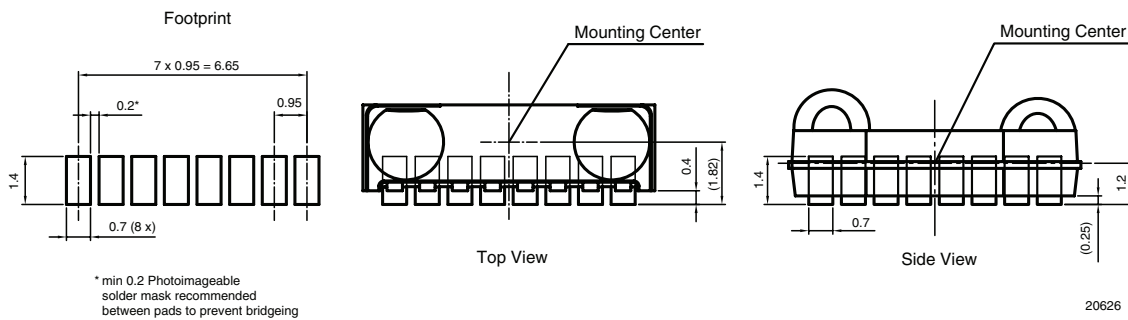
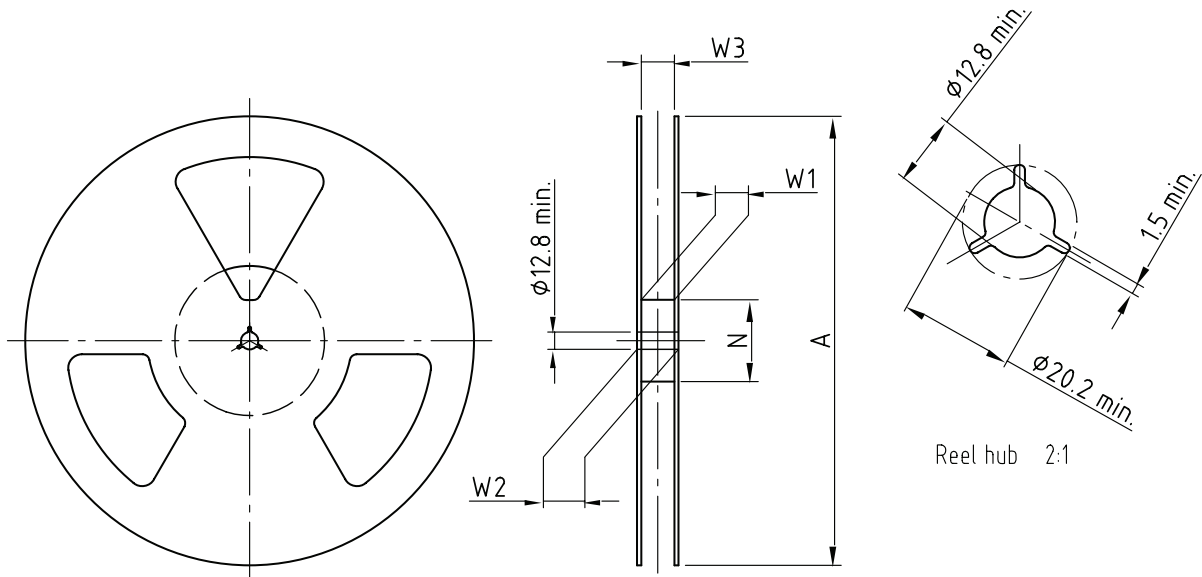


Figure 8. Package Drawing

**Reel Dimensions** in mm



Drawing-No.: 9.800-5090.01-4  
 Issue: 1; 29.11.05  
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Form of the leave open  
 of the wheel is supplier specific.

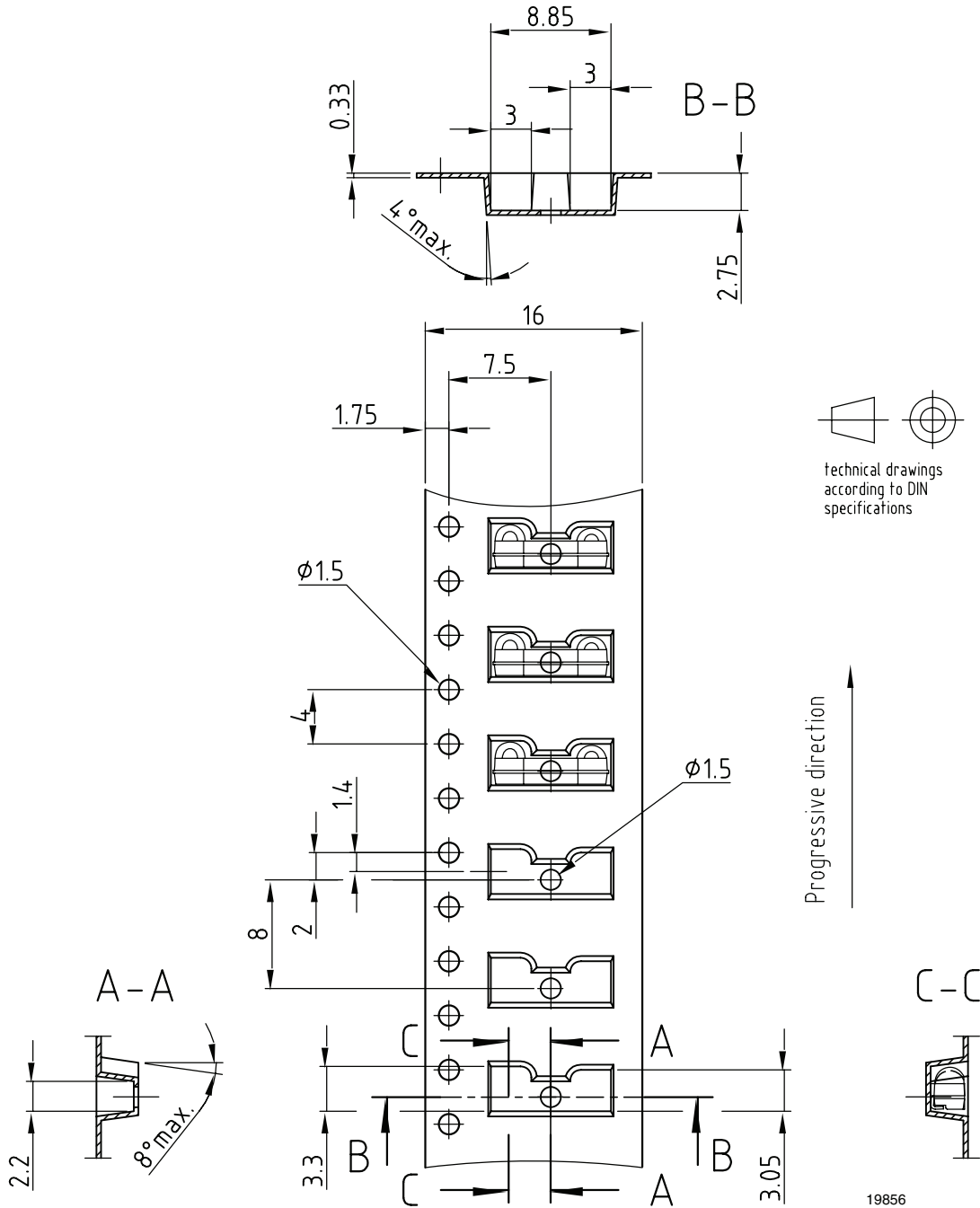
Dimension acc. to IEC EN 60 286-3

technical drawings  
 according to DIN  
 specifications

Figure 9. Reel Drawing

Tape width	A max.	N	W <sub>1</sub> min.	W <sub>2</sub> max.	W <sub>3</sub> min.	W <sub>3</sub> max.
mm	mm	mm	mm	mm	mm	mm
16	180	60	16.4	22.4	15.9	19.4
16	330	50	16.4	22.4	15.9	19.4



**Tape Dimensions** in mm


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 Issue: 1; 08.12.04

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Figure 11. Tape Drawing, TF DU6301 for Side View Mounting



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