# TP65H015G5WS

## 650V SuperGaN™ FET in TO-247 (source tab) Preliminary Datasheet

### Description

The TP65H015G5WS 650V, 15 mΩ gallium nitride GaN FET is a normally-off device using Transphorm's Gen V platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen V SuperGaN™ platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

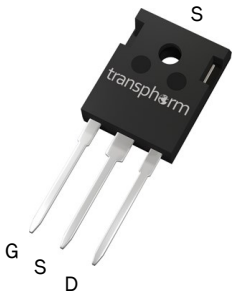
### Related Literature

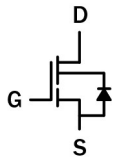
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing
- AN0010: Paralleling GaN FETs

### Ordering Information

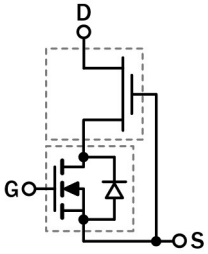
| Part Number | Package | Package Configuration |
|---|---|---|
| TP65H015G5WS | 3 lead TO-247 | Source |

**TP65H015G5WS**
**TO-247**
(top view)




**Cascode Schematic Symbol**




**Cascode Device Structure**

### Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low $Q_{RR}$
- Reduced crossover loss

### Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

### Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor

| Key Specifications | |
|---|---|
| $V_{DSS}$ (V) | 650 |
| $V_{(TR)DSS}$ (V) | 725 |
| $R_{DS(on)eff}$ (mΩ) max* | 18 |
| $Q_{RR}$ (nC) typ | 430 |
| $Q_G$ (nC) typ | 68 |

* Dynamic on-resistance; see Figures 18 and 19

## Absolute Maximum Ratings ($T_C$=25°C unless otherwise stated.)

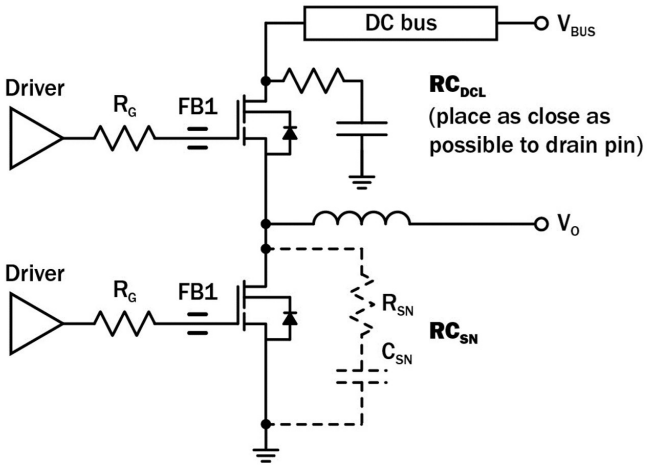
| Symbol | Parameter | | Limit Value | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to source voltage ($T_J$ = -55°C to 150°C) | | 650 | V |
| $V_{(TR)DSS}$ | Transient drain to source voltage [a] | | 725 | |
| $V_{GSS}$ | Gate to source voltage | | ±20 | |
| $P_D$ | Maximum power dissipation @$T_C$=25°C | | 276 | W |
| $I_D$ | Continuous drain current @$T_C$=25°C [b] | | 95 | A |
| | Continuous drain current @$T_C$=100°C [b] | | 60 | A |
| $I_{DM}$ | Pulsed drain current (pulse width: 10µs) | | 600 | A |
| $T_C$ | Operating temperature | Case | -55 to +150 | °C |
| $T_J$ | | Junction | -55 to +150 | °C |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_{SOLD}$ | Soldering peak temperature [c] | | 260 | °C |

Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <1µs
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. For 10 sec., 1.6mm from the case

## Thermal Resistance

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Junction-to-case | 0.45 | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient | 40 | °C/W |

## Circuit Implementation




**Simplified Half-bridge Schematic ( See also on Figure 13 )**

Layout Recommendations: ( See also AN0009)
Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

Power loop: ( For reference see page 13 )

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

Recommended gate drive: (0V, 12V) with $R_G$=15Ω

| Gate Ferrite Bead (FB1) | Required DC Link RC Snubber ($RC_{DCL}$) [a] | Recommended Switching Node RC Snubber ($RC_{SN}$) [b,c] |
|---|---|---|
| 80-120 Ω at 100MHz | [10nF + 3.3 Ω] x 3 | Not necessary |

Notes:

a. $RC_{DCL}$ should be placed as close as possible to the drain pin
b. $RC_{SN}$ is needed only if $R_G$ is smaller than recommendations or operational current exceeds 100C rated $I_{DMAX}$
c. If required, please use (100 pF + 10 ohm) or parallel two or three of the same

**Electrical Parameters** ($T_J$=25°C unless otherwise stated)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| **Forward Device Characteristics** | | | | | | |
| $V_{(BL)DSS}$ | Drain-source voltage | 650 | — | — | V | $V_{GS}$=0V |
| $V_{GS(th)}$ | Gate threshold voltage | 3.3 | 4 | 4.8 | V | $V_{DS}$=$V_{GS}$, $I_D$=2mA |
| $R_{DS(on)eff}$ | Drain-source on-resistance [a] | — | 15 | 18 | mΩ | $V_{GS}$=10V, $I_D$=60A |
| | | — | 31 | — | | $V_{GS}$=10V, $I_D$=60A, $T_J$=150°C |
| $I_{DSS}$ | Drain-to-source leakage current | — | 7 | 70 | μA | $V_{DS}$=650V, $V_{GS}$=0V |
| | | — | 50 | — | | $V_{DS}$=650V, $V_{GS}$=0V, $T_J$=150°C |
| $I_{GSS}$ | Gate-to-source forward leakage current | — | — | 400 | nA | $V_{GS}$=20V |
| | Gate-to-source reverse leakage current | — | — | -400 | | $V_{GS}$=-20V |
| $C_{ISS}$ | Input capacitance | — | 4670 | — | pF | $V_{GS}$=0V, $V_{DS}$=400V, *f*=1MHz |
| $C_{OSS}$ | Output capacitance | — | 312 | — | | |
| $C_{RSS}$ | Reverse transfer capacitance | — | 8 | — | | |
| $C_{O(er)}$ | Output capacitance, energy related [b] | — | 497 | — | pF | $V_{GS}$=0V, $V_{DS}$=0V to 400V |
| $C_{O(tr)}$ | Output capacitance, time related [c] | — | 1020 | — | | |
| $Q_G$ | Total gate charge | — | 68 | 100 | nC | $V_{DS}$=400V, $V_{GS}$=0V to 10V, $I_D$=60A |
| $Q_{GS}$ | Gate-source charge | — | 30 | — | | |
| $Q_{GD}$ | Gate-drain charge | — | 18 | — | | |
| $Q_{OSS}$ | Output charge | — | 430 | — | nC | $V_{GS}$=0V, $V_{DS}$=0V to 400V |
| $t_{D(on)}$ | Turn-on delay | — | 78 | — | ns | $V_{DS}$=400V, $V_{GS}$=0V to 12V, $R_G$=15Ω, $Z_{FB}$=120Ω at 100MHz, $I_D$=60A |
| $t_R$ | Rise time | — | 20 | — | | |
| $t_{D(off)}$ | Turn-off delay | — | 132 | — | | |
| $t_F$ | Fall time | — | 10 | — | | |

Notes:
a. Dynamic on-resistance; see Figures 18 and 19 for test circuit and conditions
b. Equivalent capacitance to give same stored energy as $V_{DS}$ rises from 0V to 400V
c. Equivalent capacitance to give same charging time as $V_{DS}$ rises from 0V to 400V

**Electrical Parameters** ($T_J$=25°C unless otherwise stated)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| **Reverse Device Characteristics** | | | | | | |
| $I_S$ | Reverse current | — | — | 60 | A | $V_{GS}$=0V, $T_C$=100°C ≤15% duty cycle |
| $V_{SD}$ | Reverse voltage [a] | — | 1.5 | — | V | $V_{GS}$=0V, $I_S$=60A |
| | | — | 1.1 | — | | $V_{GS}$=0V, $I_S$=30A |
| $t_{RR}$ | Reverse recovery time | — | 100 | — | ns | $I_S$=60A, $V_{DD}$=400V, di/dt=1000A/µs |
| $Q_{RR}$ | Reverse recovery charge | — | 430 | — | nC | |
| $(di/dt)_{RM}$ | Reverse diode di/dt [b] | — | — | 3500 | A/µs | Circuit implementation and parameters on page 3 |

Notes:
a. Includes dynamic $R_{DS(on)}$ effect
b. Reverse conduction di/dt will not exceed this max value with recommended $R_G$.

**Typical Characteristics** ($T_C$=25 °C unless otherwise stated)

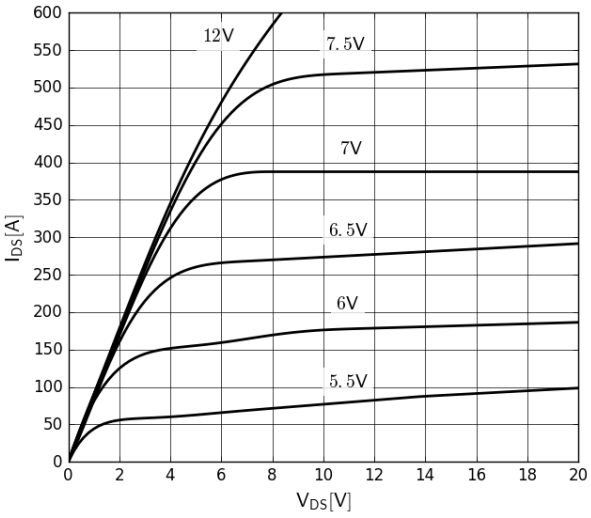



**Figure 1. Typical Output Characteristics $T_J$=25 °C**
Parameter: $V_{GS}$

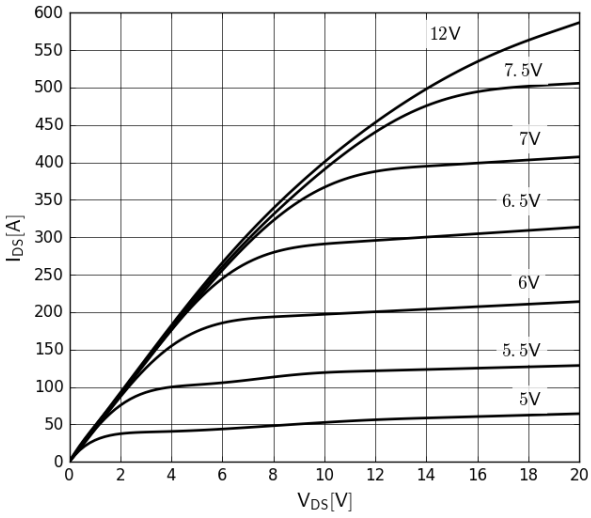



**Figure 2. Typical Output Characteristics $T_J$=150 °C**
Parameter: $V_{GS}$

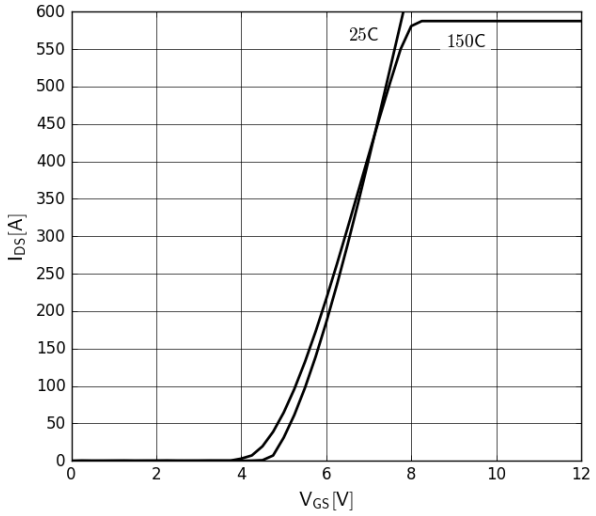



**Figure 3. Typical Transfer Characteristics**
$V_{DS}$=20V, parameter: $T_J$

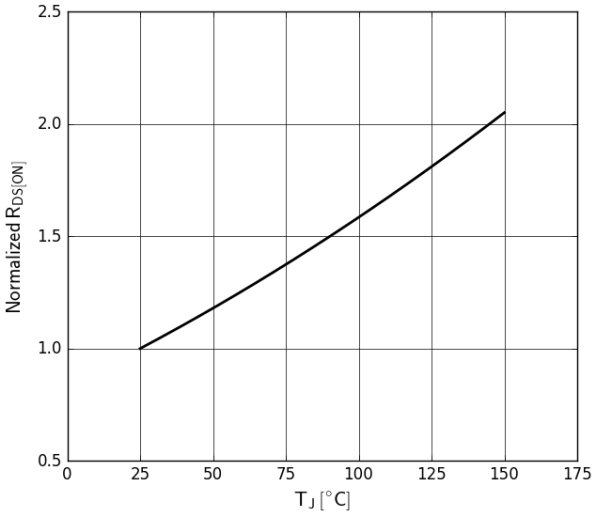



**Figure 4. Normalized On-resistance**
$I_D$=60A, $V_{GS}$=8V

**Typical Characteristics** ($T_C$=25 °C unless otherwise stated)

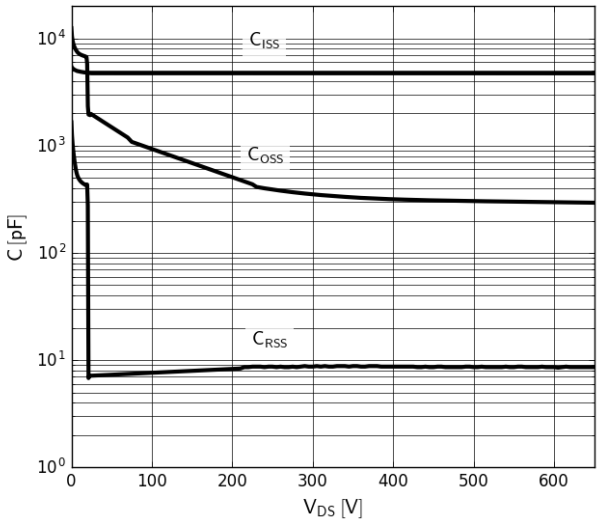



**Figure 5. Typical Capacitance**
$V_{GS}$=0V, f=1MHz

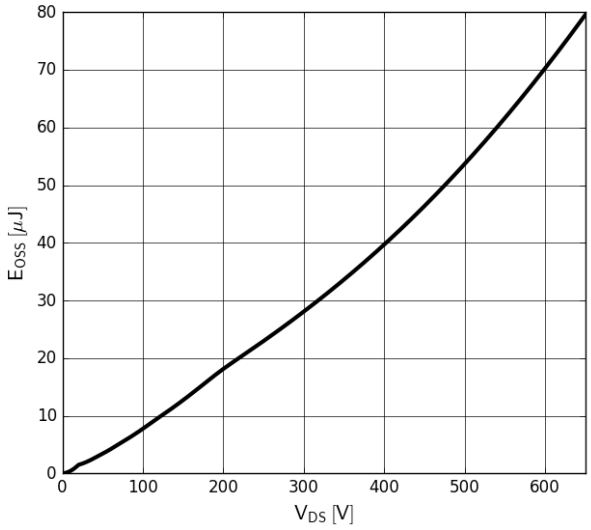



**Figure 6. Typical $C_{oss}$ Stored Energy**

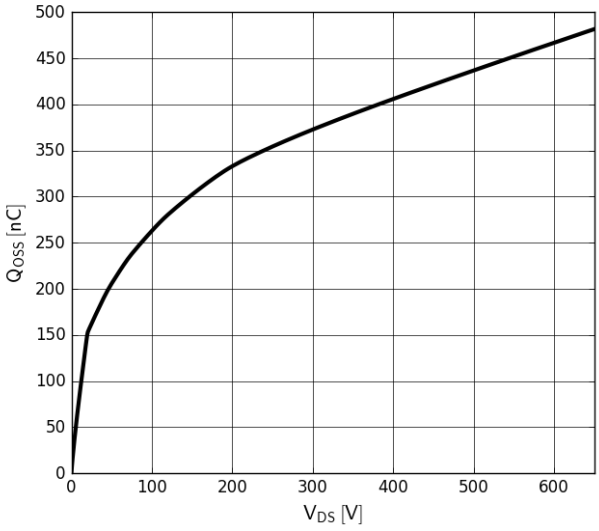



**Figure 7. Typical $Q_{oss}$**

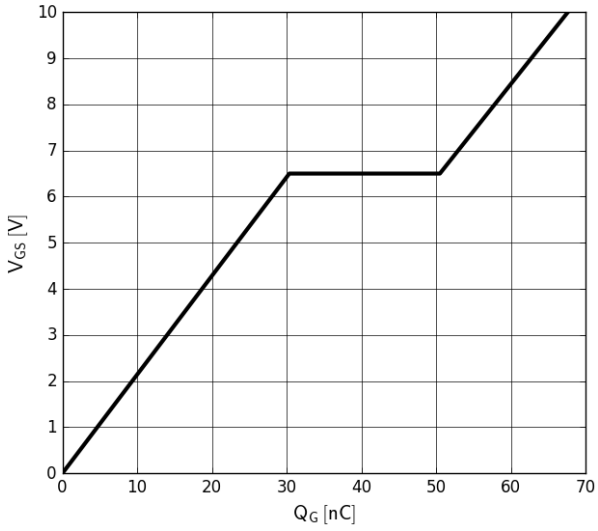



**Figure 8. Typical Gate Charge**
$I_{DS}$=60A, $V_{DS}$=400V

**Typical Characteristics** ($T_C$=25 °C unless otherwise stated)

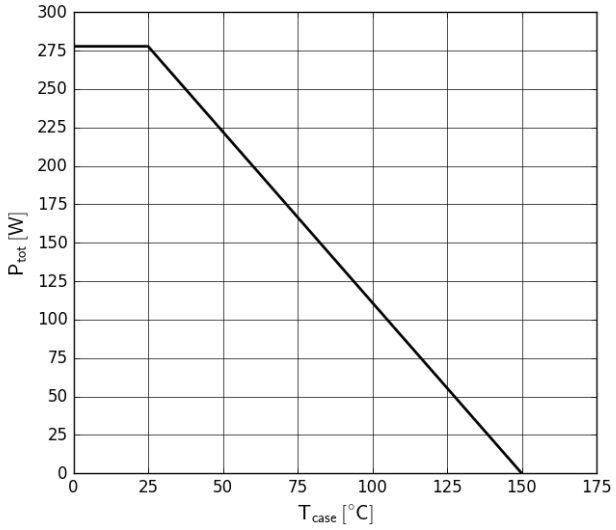



**Figure 9. Power Dissipation**

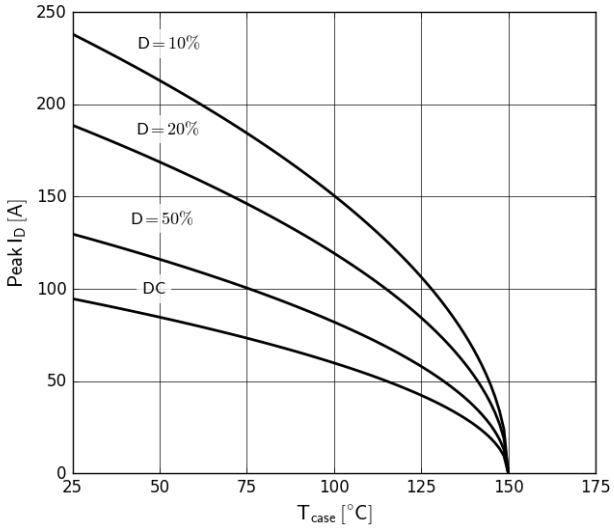



**Figure 10. Current Derating**
Pulse width ≤ 10µs, $V_{GS}$ ≥ 10V

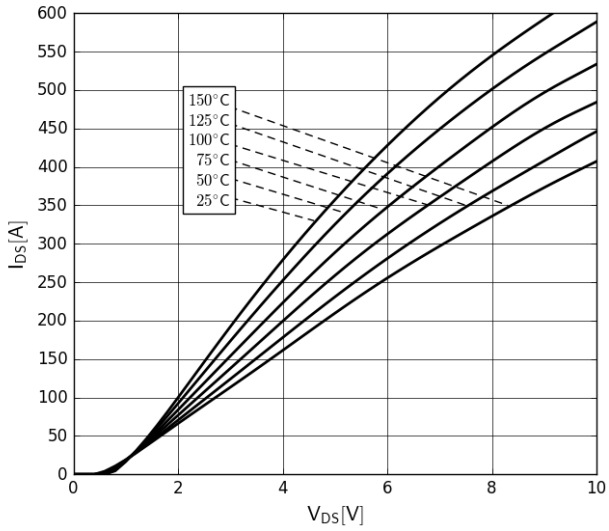



**Figure 11. Forward Characteristics of Rev. Diode**
$I_S$=f($V_{SD}$), parameter: $T_J$

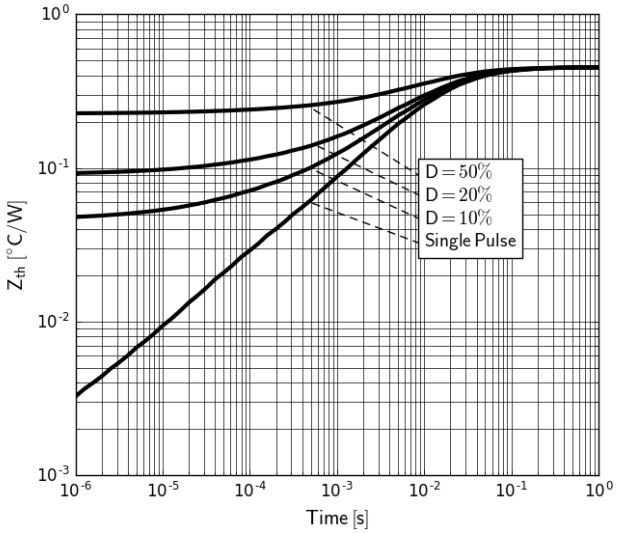



**Figure 12. Transient Thermal Resistance**

**Typical Characteristics** ($T_C$=25 °C unless otherwise stated)

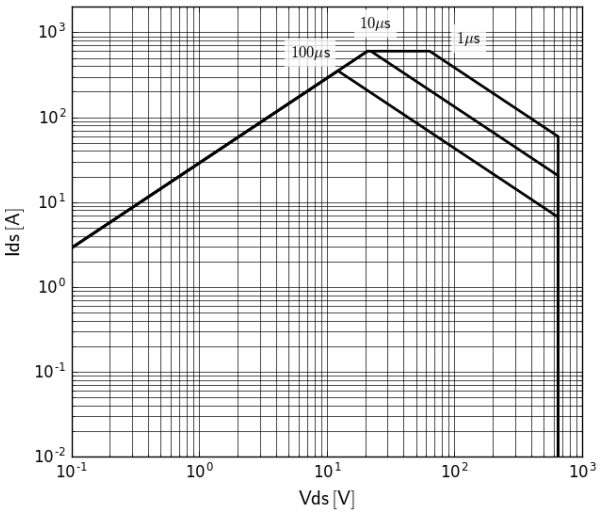



**Figure 13. Safe Operating Area $T_C$=25 °C**

## Test Circuits and Waveforms

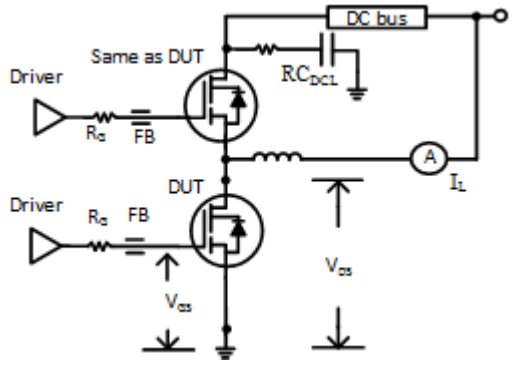



**Figure 14. Switching Time Test Circuit**
(see circuit implementation on page 3
for methods to ensure clean switching)

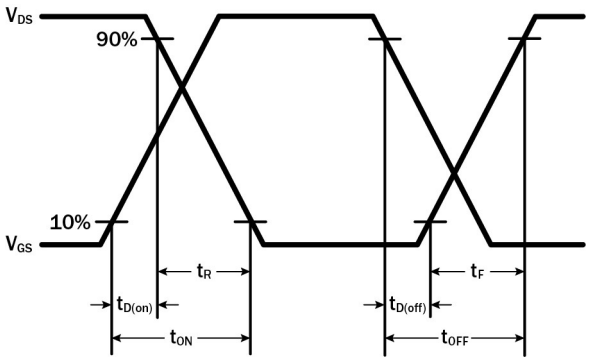



**Figure 15. Switching Time Waveform**

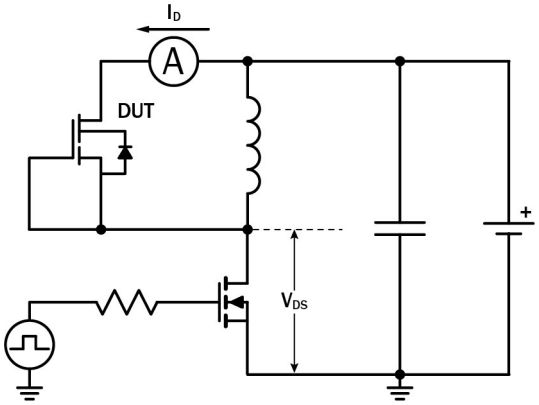



**Figure 16. Diode Characteristics Test Circuit**

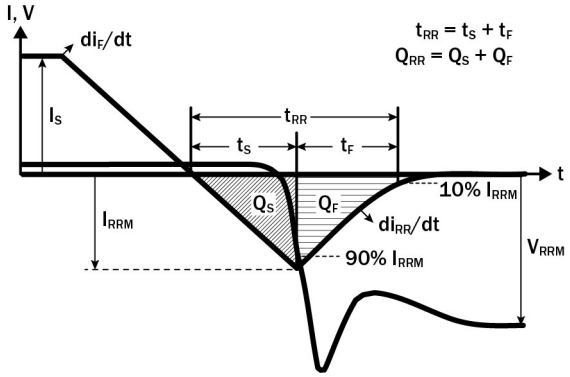



**Figure 17. Diode Recovery Waveform**

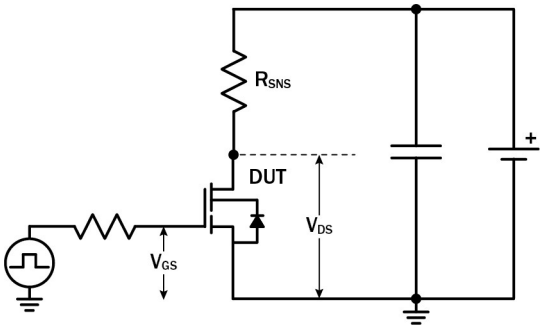



**Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit**

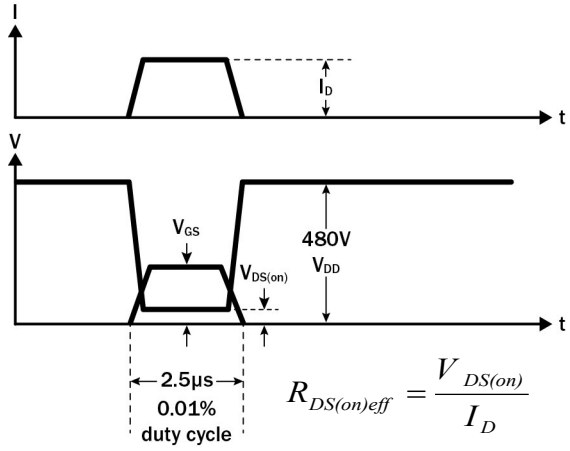



**Figure 19. Dynamic $R_{DS(on)eff}$ Waveform**

## Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

**When Evaluating Transphorm GaN Devices:**

| DO | DO NOT |
|---|---|
| Minimize circuit inductance by keeping traces short, both in the drive and power loop | Twist the pins of TO-220 or TO-247 to accommodate GDS board layout |
| Minimize lead length of TO-220 and TO-247 package when mounting to the PCB | Use long traces in drive circuit, long lead length of the devices |
| Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points | Use differential mode probe or probe ground clip with long wire |
| See AN0003: Printed Circuit Board Layout and Probing | |

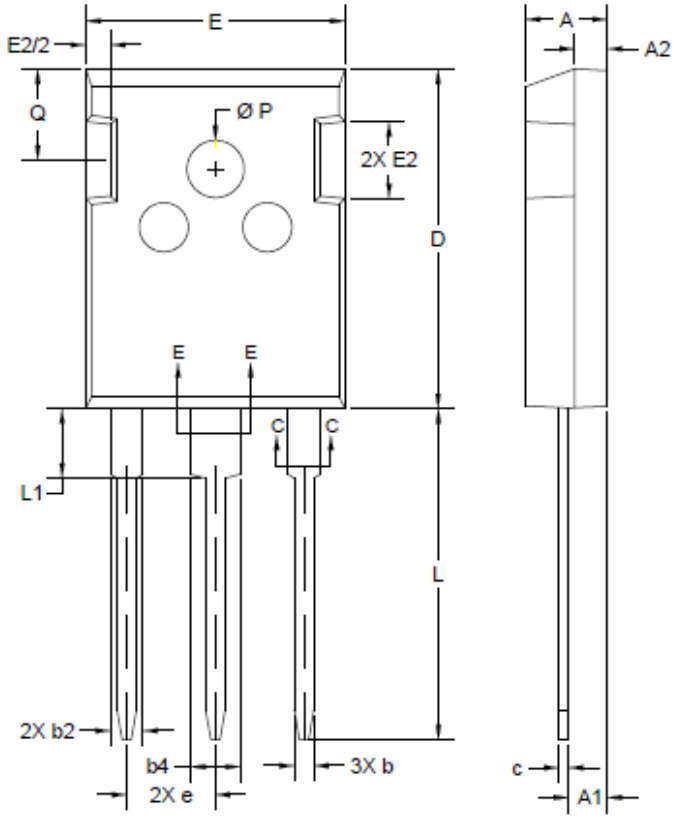
## GaN Design Resources

The complete technical library of GaN design tools can be found at transphormusa.com/design:

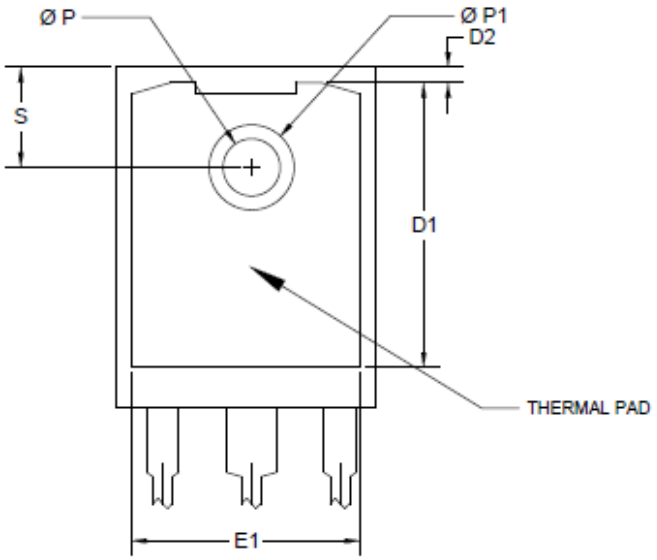
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

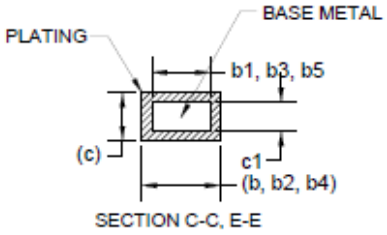
## Mechanical

## 3 Lead TO-247 Package




| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 4.82 | 5.00 | 5.19 | 0.190 | 0.197 | 0.204 |
| A1 | 2.20 | 2.39 | 2.57 | 0.087 | 0.094 | 0.101 |
| A2 | 1.82 | 2.01 | 2.18 | 0.072 | 0.079 | 0.086 |
| b | 1.09 | 1.19 | 1.35 | 0.043 | 0.047 | 0.053 |
| b1 | 1.09 | - | 1.30 | 0.043 | - | 0.051 |
| b2 | 1.87 | 2.03 | 2.31 | 0.074 | 0.080 | 0.091 |
| b3 | 1.87 | - | 2.27 | 0.074 | - | 0.089 |
| b4 | 2.94 | 3.05 | 3.22 | 0.116 | 0.120 | 0.127 |
| b5 | 2.94 | - | 3.18 | 0.116 | - | 0.125 |
| c | 0.50 | 0.58 | 0.68 | 0.020 | 0.023 | 0.027 |
| c1 | 0.50 | - | 0.64 | 0.020 | - | 0.025 |
| D | 20.67 | 20.85 | 21.11 | 0.814 | 0.821 | 0.831 |
| D1 | 17.20 | - | 17.63 | 0.677 | - | 0.694 |
| D2 | 0.81 | - | 1.20 | 0.032 | - | 0.048 |
| E | 15.72 | 15.90 | 16.15 | 0.619 | 0.626 | 0.636 |
| E1 | 13.79 | - | 14.25 | 0.543 | - | 0.561 |
| E2 | 4.30 | - | 4.86 | 0.169 | - | 0.191 |
| e | 5.46 BSC | | | 0.215 BSC | | |
| L | 19.55 | 19.94 | 20.38 | 0.770 | 0.785 | 0.802 |
| L1 | 3.93 | 4.11 | 4.48 | 0.155 | 0.162 | 0.176 |
| ØP | 3.50 | 3.61 | 3.69 | 0.138 | 0.142 | 0.145 |
| ØP1 | 7.08 | 7.19 | 7.32 | 0.279 | 0.283 | 0.288 |
| Q | 5.41 | - | 5.85 | 0.213 | - | 0.230 |
| S | 6.15 BSC | | | 0.242 BSC | | |



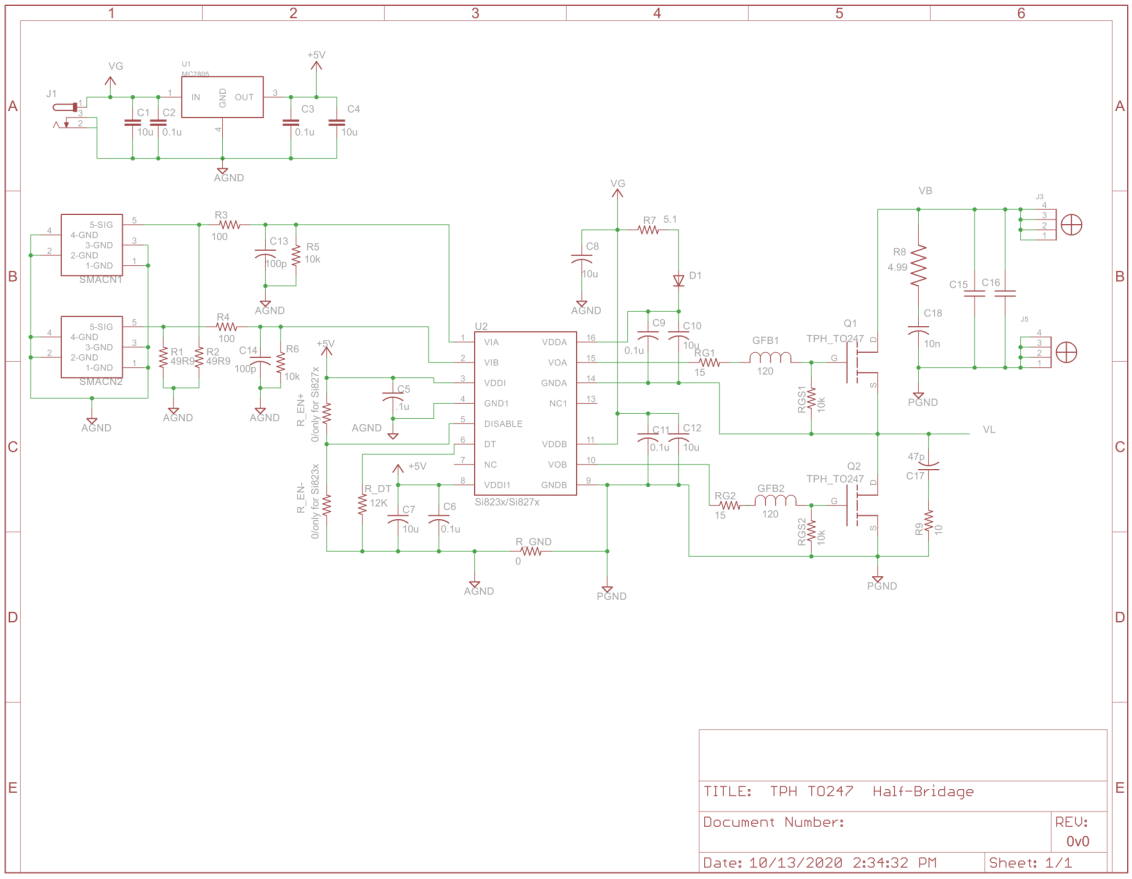




NOTES:

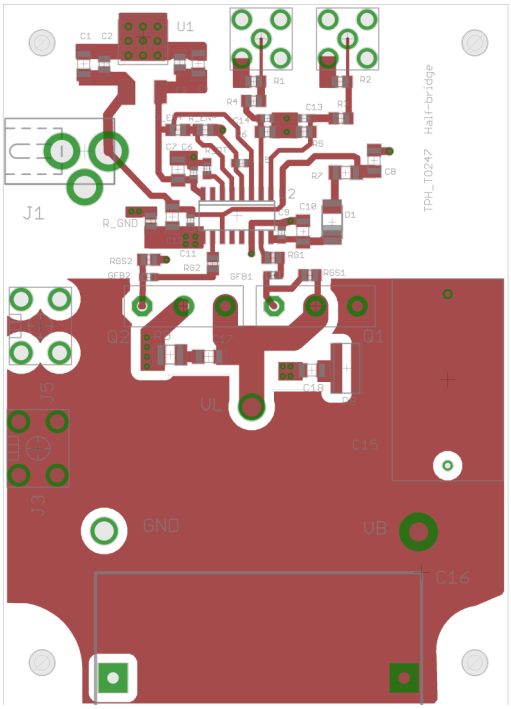
1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.
3. LEAD FINISH UNCONTROLLED IN L1.
4. OUTLINE CONFORMS TO JEDEC TO-247AD.

| TO-247 3L | | | |
|---|---|---|---|
| transphorm | | | |
| SCALE: 1:1 | SHEET 1/1 | DRAWING NO. 200019 | VER. 3 |

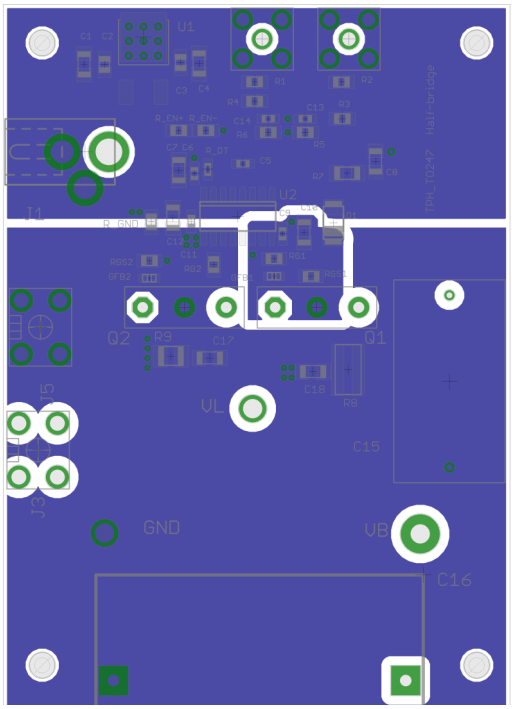
## Half-bridge Reference Schematic and PCB Layout




**Half-bridge layout Sample (Top Layer)**



**Half-bridge layout Sample (Bottom Layer)**



## Revision History

| Version | Date | Change(s) |
|---|---|---|
| 0.1 | 5/25/2020 | Preliminary Datasheet |
| 0.2 | 9/24/2020 | Preliminary Datasheet |
| | | |
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