High Brightness LED Driver

Features

- Input voltage range from 5V to 450V
- Constant off time control
- Line compensation of output current
- Enable pin
- Leading-edge blanking
- Frequency modulation in short circuit protection and low output voltage condition
- Over-temperature protection
- Over-current protection
- SOP-8 package, with few external components needed

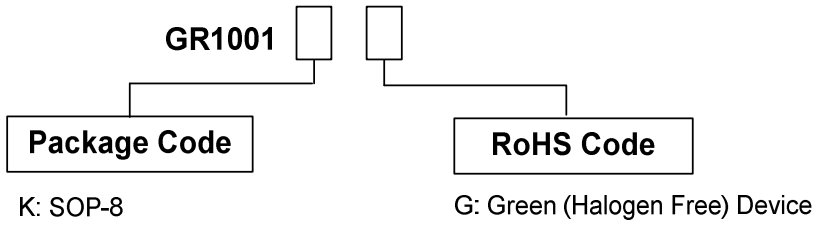
Application

- LED Lighting

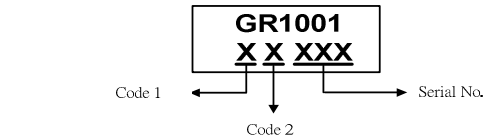
General Description

The GR1001 is a high brightness LED driver. A high voltage power NMOSFET, BV_{DSS} is 600V, as the high side device and the power NMOSFET inside the GR1001 as the low side device in this topology. A Zener voltage, was generated by ST pin of the GR1001, turn on the high side device all the time by connected to the gate terminal of the high side device. The source terminal and the drain terminal of the high side device are connected to the DRN pin of the GR1001 and the input voltage rail respectively to absorb the very large voltage potential. The current peak value was decided by the sensing resistor in the CS pin, the low side device was turned off by the current peak detection then delay a fixed off time that set by the resistor in the RT pin of GR1001.

Ordering and Marking Information



SOP-8



Code 1	8	9	A	B		G	H	I	J
Year	2008	2009	2010	2011		2016	2017	2018	2019
Code 2	1	2	3	4		9	A	B	C
Month	Jan.	Feb.	Mar.	Apr.		Sep.	Oct.	Nov.	Dec.

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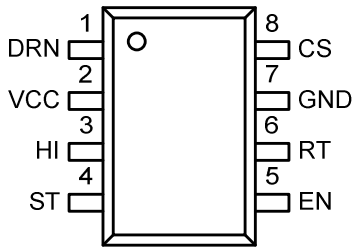
Pin Configuration

TOP VIEW



Pin Description

Pin No.	Name	Function
1	DRN	The drain terminal of the internal NMOSFET.
2	VCC	The output of the internal regulator.
3	HI	This pin pull high
4	ST	The anode terminal of the internal Zener diode.
5	EN	The enable input terminal.
6	RT	An external resistor located from this pin to GND to generate a reference current to fix the off time in the switching operation.
7	GND	Ground of the circuit.
8	CS	Current sense voltage input terminal, the LED current also flows from this pin to the sense resistor outside.

Absolute Maximum Ratings

Supply voltage, V_{CC} ---------- 5.5V

Drain voltage, V_{DRN} ---------- 26V

Zener voltage, V_{ST} ---------- 18V

EN voltage to GND, V_{EN} ---------- -0.3V ~ 6V

RT voltage to GND, V_{RT} ---------- -0.3V ~ 6V

CS voltage to GND, V_{CS} ---------- -0.3V ~ 6V

Junction temperature ---------- 150°C

Operating ambient temperature ---------- -20°C ~ 85°C

Storage temperature range ---------- -65°C ~ 150°C

Package thermal resistance (SOP-8), θ_{JA} ---------- 160°C/W

Power dissipation (SOP-8, at ambient temperature = 85°C) ---------- 400mW

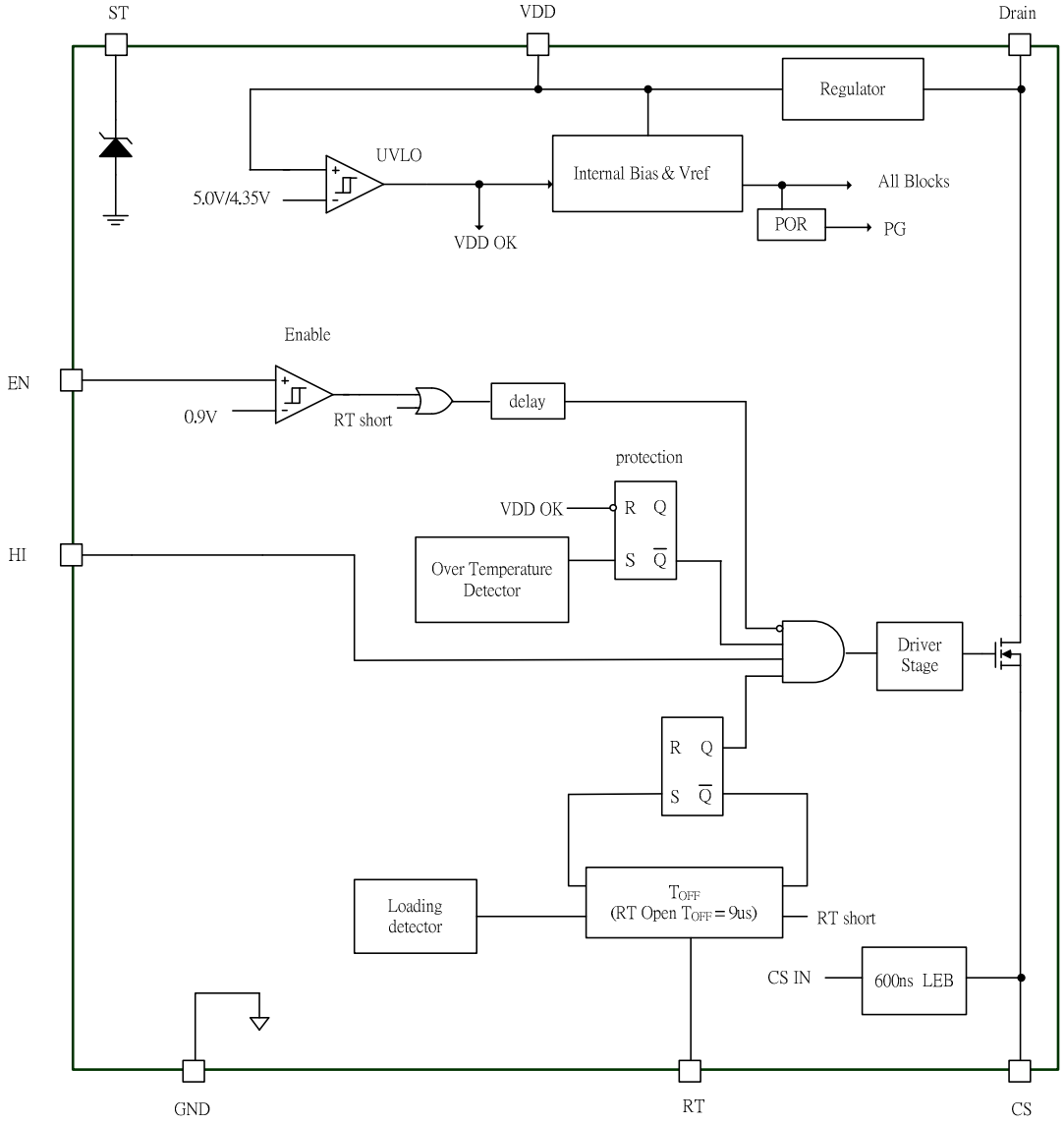
Lead temperature (Soldering, 10sec) ---------- 260°C

Recommended Operating Conditions

Item	Min.	Max.	Unit
Input voltage, V_{IN} *	5	450	V
Output current, I_{OUT} *	0.1	0.8	A

* Refer to the Figure-1.

Block Diagram



Electrical Characteristics (V_{CC} = 5V, T_A = 25℃, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
INPUT VOLTAGE						
Input voltage range	V_{IN}	With Cascode NMOSFET	5	-	450	V
VCC SECTION						
V_{CC} UVLO	V_{UVLO}		4.8	5.0	5.2	V
V_{CC} UVLO hysteresis	$V_{UV\ LOHY}$			0.65		V
Operation current	I_{Q-OP}	Normal Operation	0.3	0.5	0.9	mA
ST SECTION						
Start up voltage in normal operation	V_{ST}	I_{ST} = 50μA	12	15	18	V
Start up current at 156V	I_{ST}	V_{IN} = 156V, R_{ST} = 2MΩ	50	70.5	90	μA
CURRENT SENSE SECTION						
Peak current reference voltage	V_{CS1}	V_{IN} = 312V,. L = 4.7μH, R_{LOAD} = 10Ω, R_{CS} = 0.3Ω	200	250	300	mV
Leading edge blanking time	T_{LEB}		500	600	700	ns
INTERNAL POWER NMOSFET SECTION						
Turned on resistance	$R_{DS(ON)}$	V_{CC} = 5V, V_{CS} = 0.1V, R_{DRN} = 10KΩ from VIN to DRN		1		Ω
EN SECTION						
Enable threshold	V_{EN}		0.85	0.9	0.95	V
Enable function hysteresis	V_{EN_HYS}			0.1		V
Delay cycles of enable pin	T_{EN_D}			32		Cycles
RT SECTION						
RT threshold voltage	V_{RT}	V_{CC} = 5V, R_{RT} = 200KΩ	1.14	1.2	1.26	V
Constant off time	T_{OFF}	V_{CC} = 5V, R_{RT} = 200KΩ	20.5	22.5	24.5	μs
Constant off time	$T_{OFF\_default}$	V_{CC} = 5V, RT to V_{CC}	9	10	11	μs
OVER TEMPERATURE PROTECTION SECTION						
OTP trip level	T_{OTP}			150		℃
OTP hysteresis	T_{OTP_HYS}			25		℃

Application Information

Operation

GR1001 is a constant current PWM converter for high brightness LED driving. In the Figure-1, after the V_{IN} ramps up, the V_{ST} also ramps up to the target with a delay time. This voltage turns on the M_1 when its level greater than the V_{TH_M1}, then the V_{CC} was created. M_2 was turned on in the on period of the first cycle. The current flows through LEDs, L_1, M_1, M_2, R_S, and back to C_{IN} finally. In the end of this period, the M_2 might be to turn off when the V_{CS} reached 0.25V. A fixed off time was followed as the off period of the first cycle. During the off period, the current flows through LEDs, L_1 and D_1. A new cycle will start when the fixed off time finish.

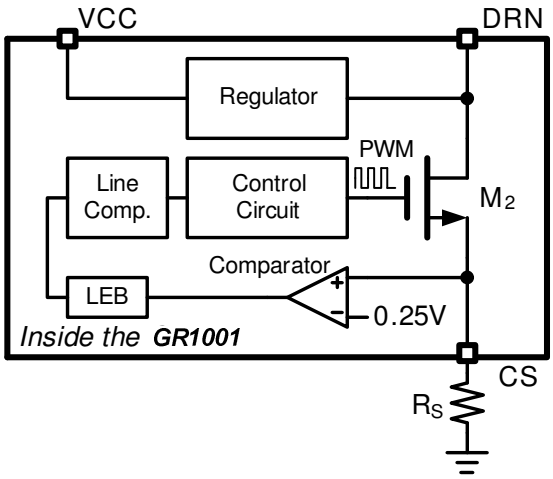


Figure-1 The brief schematic to explain the system operation.

Start Up Function

The waveforms of Figure-2 explain the power on procedure in the GR1001 application circuit. The V_{ST} created slowly due to the large time constant, T_{ST}, that formed by R_{ST} and C_{ST}. The reasonable ranges of R_{ST} and C_{ST} are 1MΩ to 10MΩ and 0.1μF to 1μF respectively. A large resistance could limit the dissipated current under hundreds microampere

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These two sets of components value affect the T_{ST} in the range of hundreds millisecond to thousands millisecond. The T_{ST} order is available defined by the user. The ceramic type of capacitor is suitable for V_{ST} regulation.

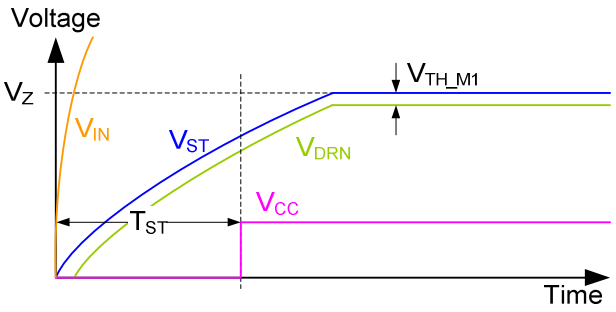


Figure-2 The start up waveforms, the voltage designators assigned in Figure-1.

V_{CC} Regulator

An internal regulator in the GR1001 could generate a 5V voltage source to supply the operating current for control circuit. The input voltage of the internal regulator is the V_{DRN}. V_{CC} regulated in the M_2 off period due to the V_{DRN} is approximately zero volt in the M_2 on period. Therefore, a capacitor, shown in the Figure-1, located to the VCC to hold on the V_{CC} during the M_2 on period is necessary. The ceramic type of capacitor is suitable for V_{CC} retaining, a 1μF capacitor could supply the operating current of the control circuit for tens microsecond with a very good voltage regulation.

Application Information (Cont.)

Peak Current Detection and Line Voltage Compensation

In the Figure-3, a current flow through M_2 and R_S during the M_2 on period. This current caused the V_{CS} increasing, the comparator pass the peak current information to the control circuit to turn off M_2 while V_{CS} reach to 0.25V. The peak, I_{PK}, current could determine by (1):

$$I_{PK} = \frac{0.25}{R_S} \qquad (1)$$

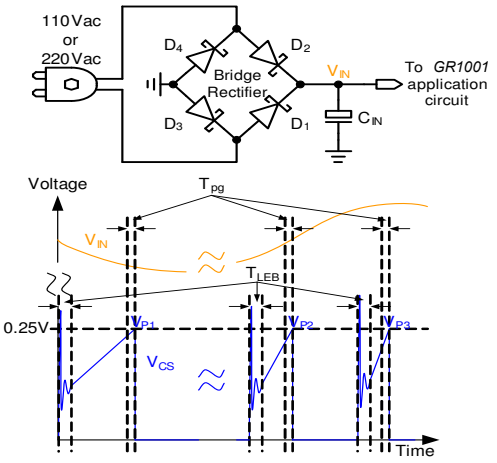


Figure-3 The brief schematic to explain the peak current detection and line voltage compensation.

In the Figure-4, there are large voltage spike in the turn on edge of V_{P1} to V_{P3}. These voltage spikes probably affect the wrong peak current detection. To prevent this fault, a LEB block applied in the GR1001 to generate a fixed period to blank the voltage spike in the CS.

The T_{pg} in the Figure-4 is the propagation delay of M_2 turned off. The T_{pg} was defined from the V_{CS} reaching 0.25V to M_2 turned off. In theT_{pg} period, the V_{CS} still ramps up from 0.25V due to the M_2 was not turned off yet. For that reason, the end of V_{CS} in the higher V_{IN} is greater than the end of V_{CS} in the lower V_{IN}.

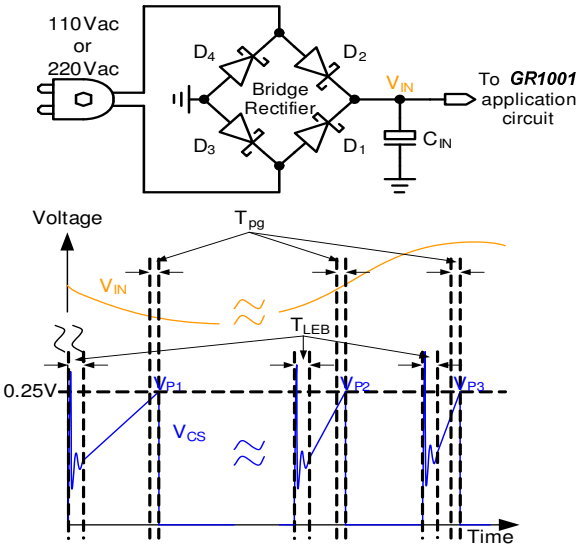


Figure-4 The waveforms of V_{IN} and V_{CS} to explain the operation of T_{LEB} and line voltage compensation. The sketch map explains the generation of V_{IN} and the line voltage change of V_{IN} due to the limited C_{IN}.

The different height of V_{CS} means the different I_{OUT} that shown in the Figure-1. The line voltage compensation function was applied in the GR1001 to improve the output current regulation. The V_{P1} to V_{P3} in the Figure-4 illustrates the compensation results by the line voltage compensation.

OFF Time Setting

GR1001 operates with the peak current sensing and the constant off time. The peak current sensing and the line voltage compensation align the peaks of V_{CS} identically to determine the same I_{PEAK} that shown in the Figure-5. The I_{VALLEY} was determined by the T_{OFF}. GR1001 provides an off time setting function via connect a resistor from RT to GND. A simple way is connect RT to VCC directly to use the default off time that the value is approximately 9.3μs.

Application Information (Cont.)

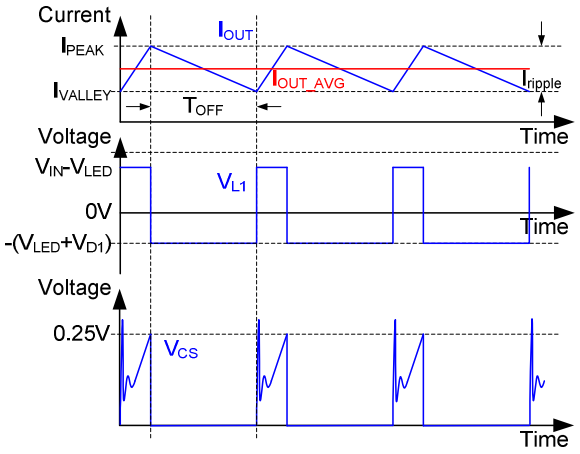


Figure-5 The waveforms of V_{CS}, V_{L1} and I_{OUT} that shown in the Figure-1.

Inductor Selection and Output Current Setting

The (2) and (3) were generated according to the Figure-5. They usually used to determine the inductance of the power inductor.

$$I_{ripple} = I_{OUT} \cdot K \quad (2)$$

$$L = \frac{(V_{LED} + V_{D1})}{I_{ripple}} \cdot T_{OFF} \quad (3)$$

Where, the I_{OUT} is output current that user defined, the K. is the percentage of I_{OUT} to estimate the worse case and the value usually is range of 20%~40%. Beside, the maximum rate current and saturation current of the inductor must greater than the I_{PEAK} that shown in the Figure-5.

The (4) to (6) could be used to estimate the capacitance of C_{IN} that shown in the Figure-1.

$$T_{CHG} = \frac{8.333m}{2} \cdot \left[1 - \frac{\sin^{-1}\left(1 - \frac{\Delta V}{V_{IN}}\right)}{90} \right] \quad (4)$$

$$T_{DIS} = 8.333m - T_{CHG} \quad (5)$$

$$C_{IN} = \frac{0.5 \cdot I_{OUT} \cdot T_{DIS}}{\Delta V} \quad (6)$$

Note that, the ΔV is the input voltage ripple that defined by the users, the T_{CHG} is the charging period and the T_{DIS} is the discharging period. In the other considerations, the maximum rate voltage of the C_{IN} must be greater than the peak value of V_{IN}, the maximum RMS current of C_{IN} must be greater than half I_{OUT}.

EN Function (Brown IN/OUT Operation)

The EN pin provides a control function to the users. The users can turn off the operation by apply a TTL logic signal via the EN pin.

Beside, EN pin can also used as a Brown IN/OUT function to make sure the operation under the suitable input voltage. In the lower input voltage, the GR1001 could stop operation via the brown in detection. The GR1001 detects the input voltage information by a voltage divider as shown in the Figure-8.

$$R_{BRN2} = \frac{0.9}{I_{BRN}} \quad (7)$$

$$R_{BRN1} = \frac{V_{IN\_BRN} \cdot R_{BRN2}}{0.9} - R_{BRN2} \quad (8)$$

(7) and (8) can be used to estimate the resistance of the R_{BRN1} and R_{BRN2}. Note that, the I_{BRN} is the acceptable current by the users, the V_{IN_BRN} is the brown in voltage threshold set by the users.

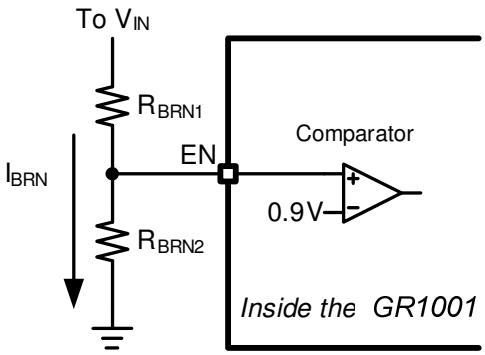


Figure-6 The sketch map of Brown In/Out setting.

Application Information (Cont.)

Over Temperature Protection (OTP)

The GR1001 provides an inner over temperature protection function to prevent the system damage. In some abnormal situation, a high temperature could trip the OTP to latch off the GR1001. The users should power on again to reset this latch.

Short Circuit Protection

In the Figure-7, the I_{OUT} runs away due to the I_{VALLEY} always higher than I_{PEAK} in the short circuit conditions. To prevent this situation, the GR1001 could increase the T_{OFF} by product a multiplier to control the I_{VALLEY} stay below I_{PEAK}. The multiplier might be 2, 4 and 8 that decided by the GR1001 control scheme.

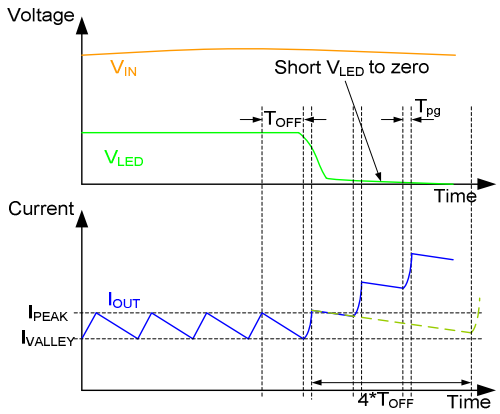


Figure-7 The sketch waveforms to illustrate the short circuits protection.

PCB Layout Consideration

Figure-8 shows the PCB layout considerations of GR1001. These guidelines detailed below.

(1) Locate the U_1, R_S, C_{IN}, D_5, L_1 and M_1 closely each other to reduce the current loop of on period and off period.

(2) Locate the R_S, C_1 and C_{ST} close to the GR1001 as possibly.

(3) Locate the M_1 to the GR1001 close as possibly to reduce the distance between the source terminal of M_1 and pin1 of U_1.

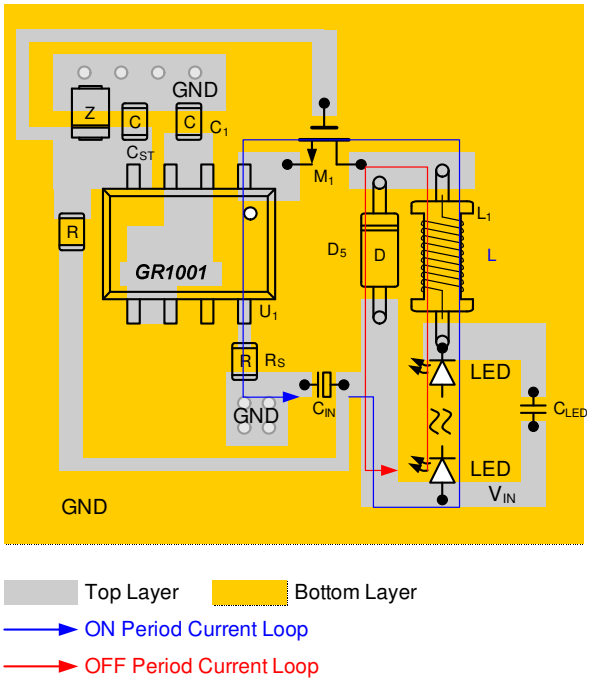


Figure-8 The PCB layout sketch map shown the layout considerations and the relative locations of the key components.

Typical Application Circuit

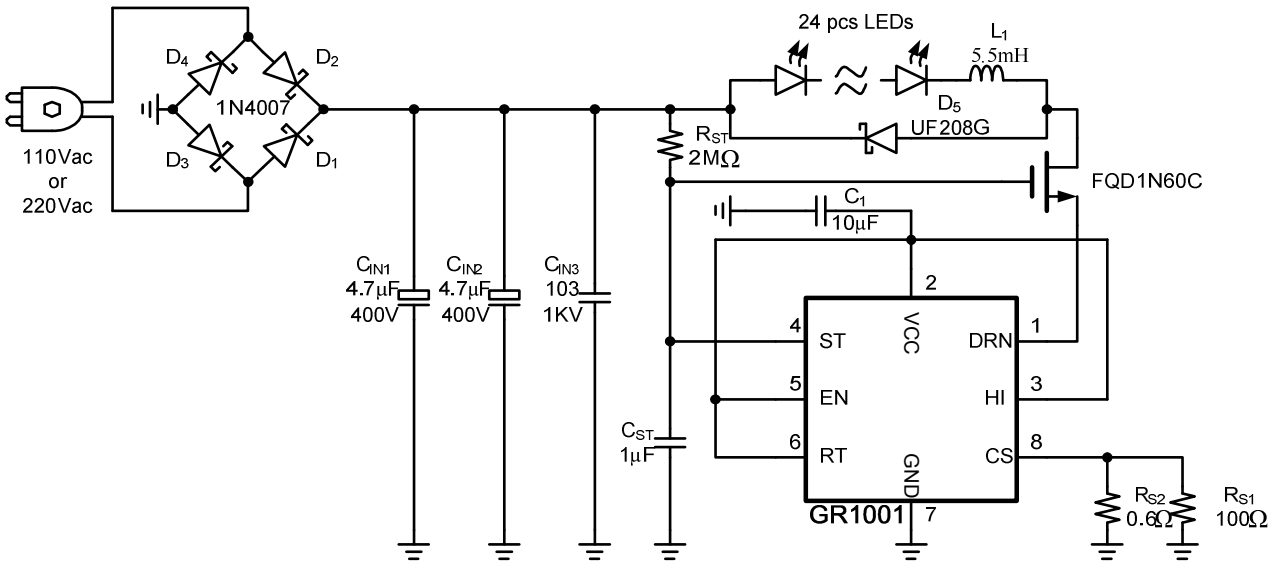
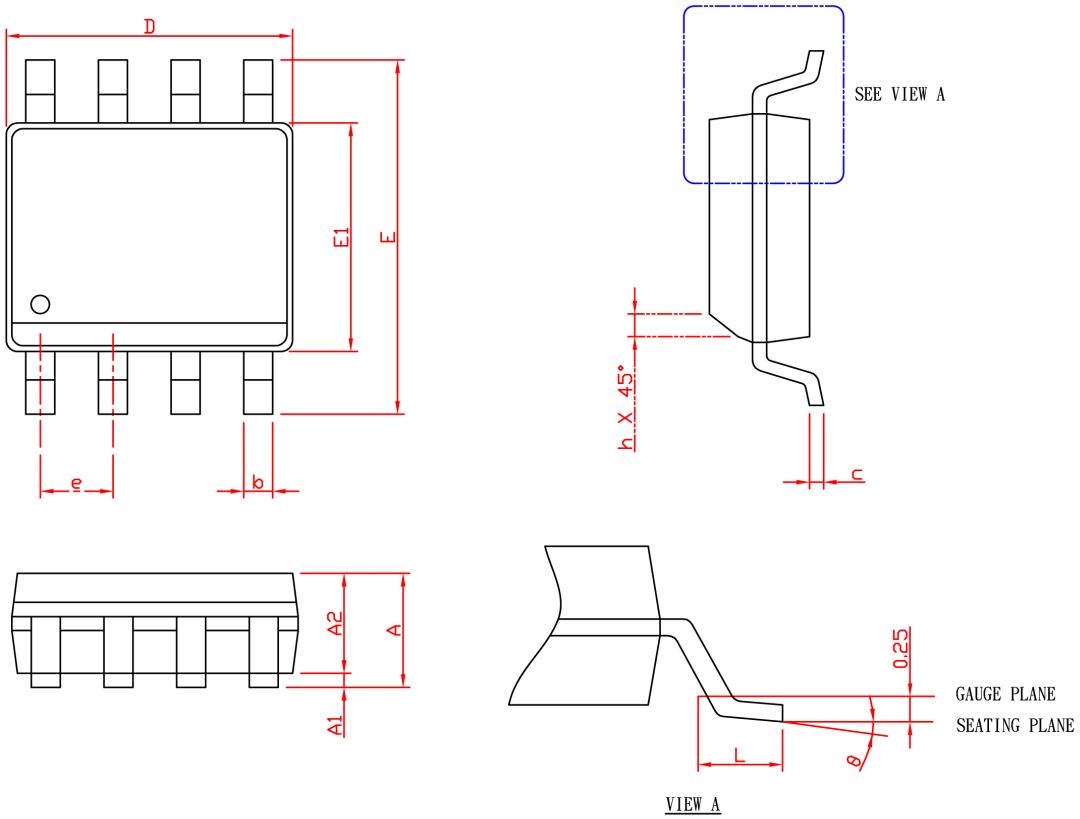


Figure-11 110Vac or 220Vac input voltage, default off time, 24pcs LEDs light bar, 350mA application circuit.

Package Information



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

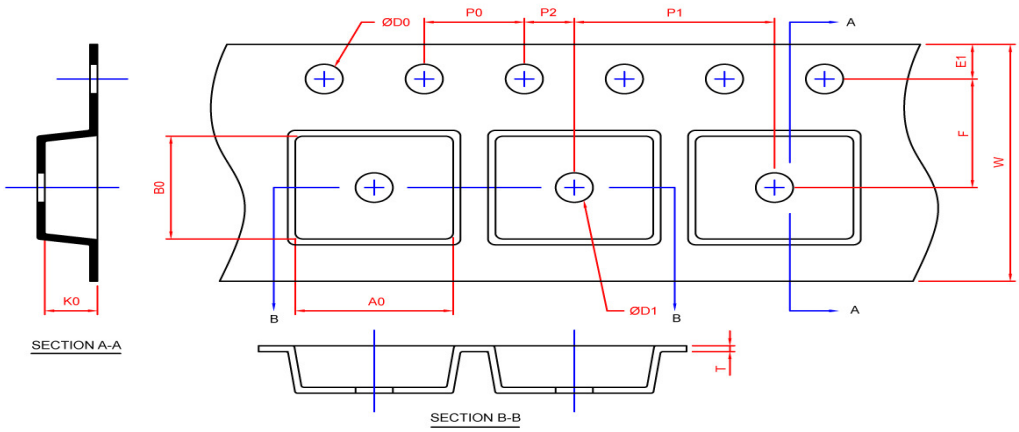
Note: 1. Followed from JEDEC MS-012 AA.

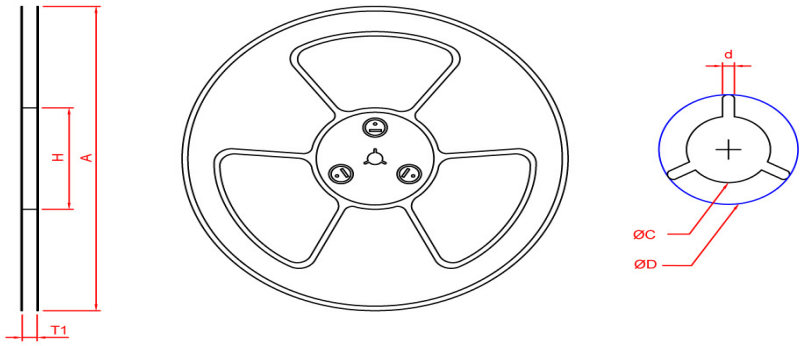
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension “E1” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions

SOP- 8





Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.0	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	-	2500

Tape and Reel Specifications

Sop-8